Electronic Circuits /1/

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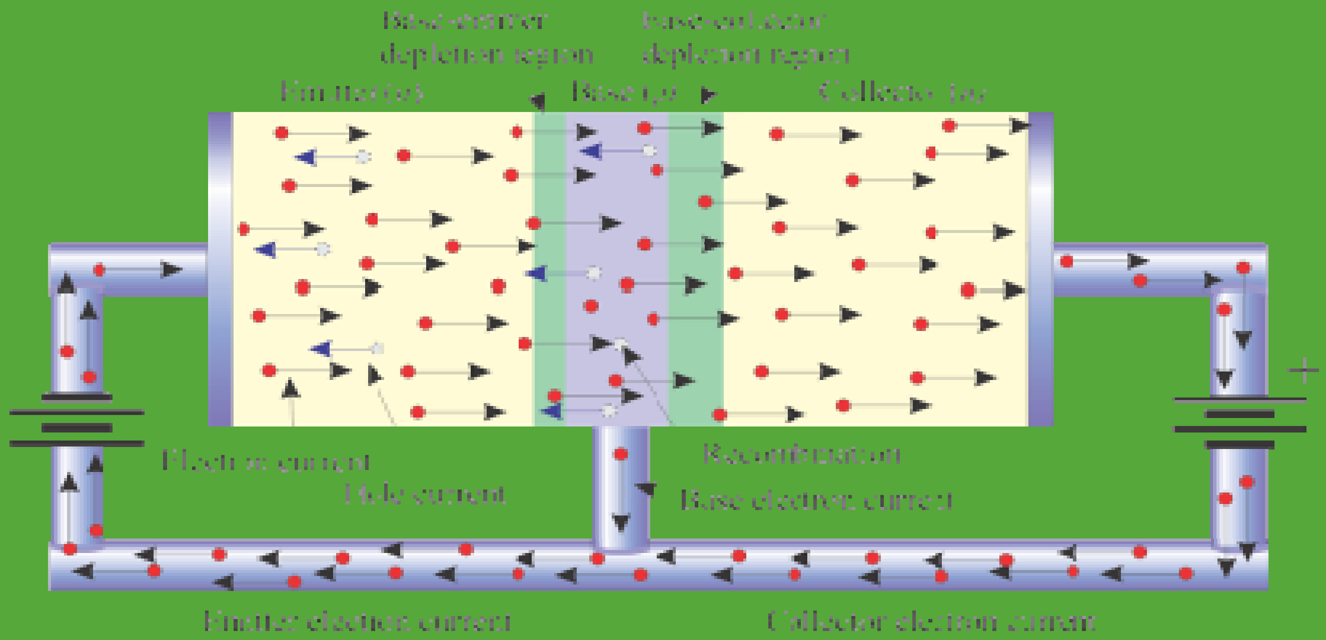
Chapter 5: ***Bipolar Junction Transistor***



Bipolar Junction Transistor

1. Introduction

During the period 1904 to1947, the vacuum tube was the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the *control grid*, to the vacuum diode, resulting in the first amplifier, the *triode*. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and the five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance, and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this

The advantages of this three-terminal solid-state device over the tube were immediately obvious:

It was smaller and lightweight; it had no heater requirement or heater loss; it had a rugged construction; it was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note that this chapter is our first discussion of devices with three or more

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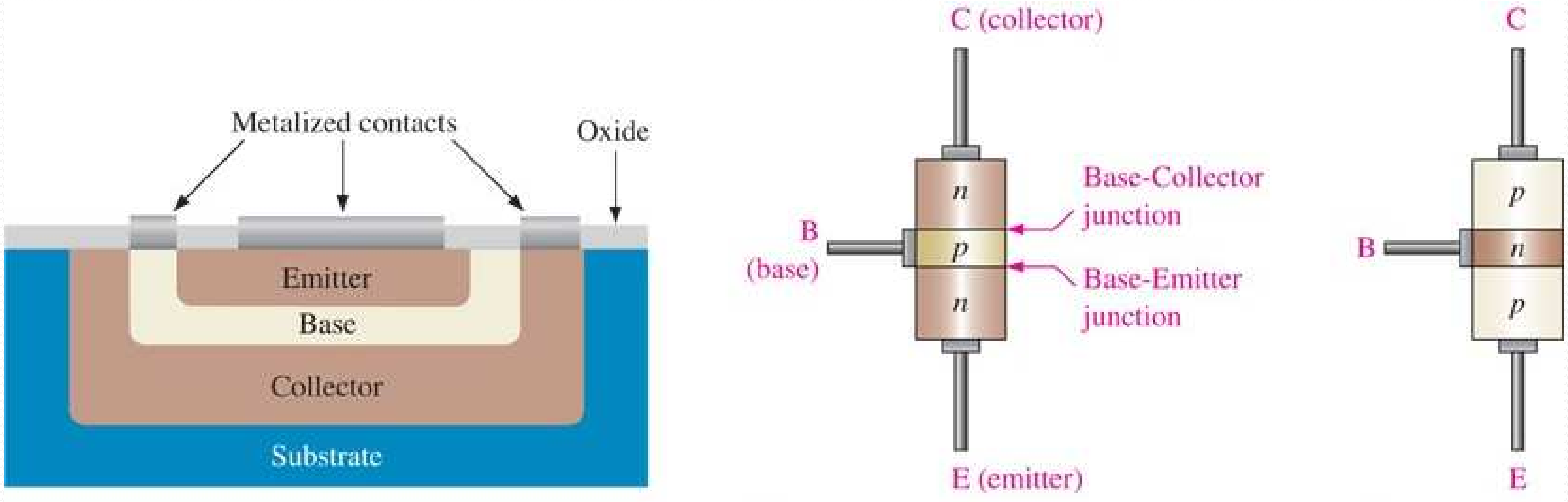
2. Transistor Construction

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor*, and the latter is called a *pnp transistor*.

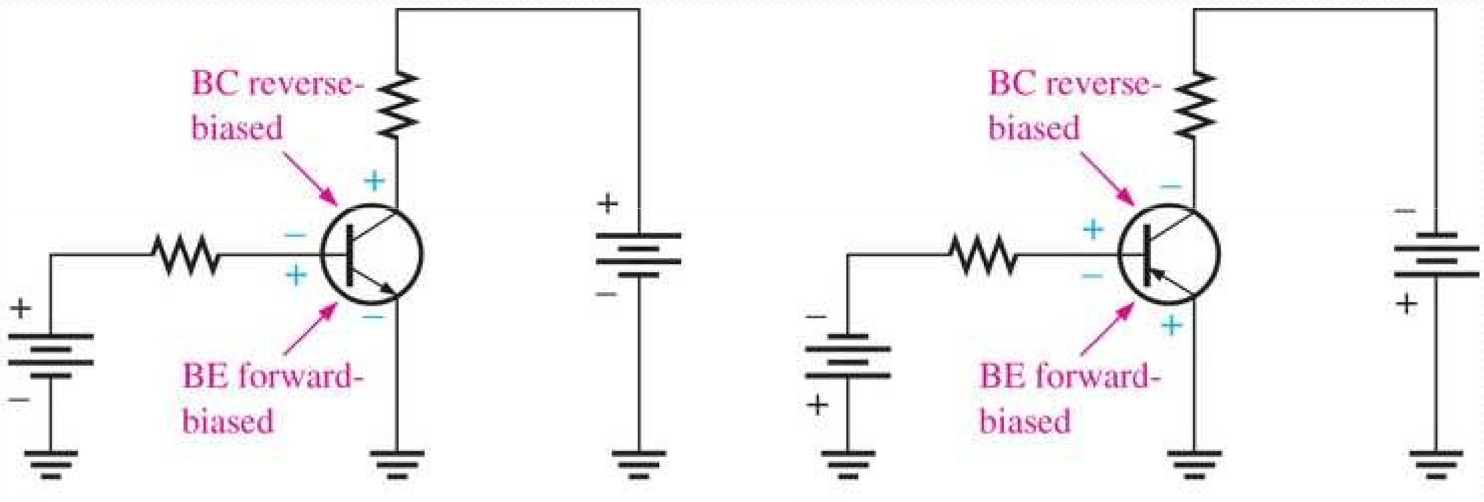


(a) Basic epitaxial planar structure (b) *npn* (c) *pnp*

The base is a thin lightly doped region compared to the heavily doped emitter and moderately doped collector regions.

3. Basic Transistor Operation

In normal operation (properly as an amplifier), the base-emitter junction is forward-biased and the base-collector junction is reverse-biased.



(a) *npn* (b) *pnp*

We mainly use the *npn* transistor for illustration. The operation of the *pnp* transistor as for the *npn* transistor except that the roles of the electrons and holes, the bias voltage polarities, and the current directions are all reversed.

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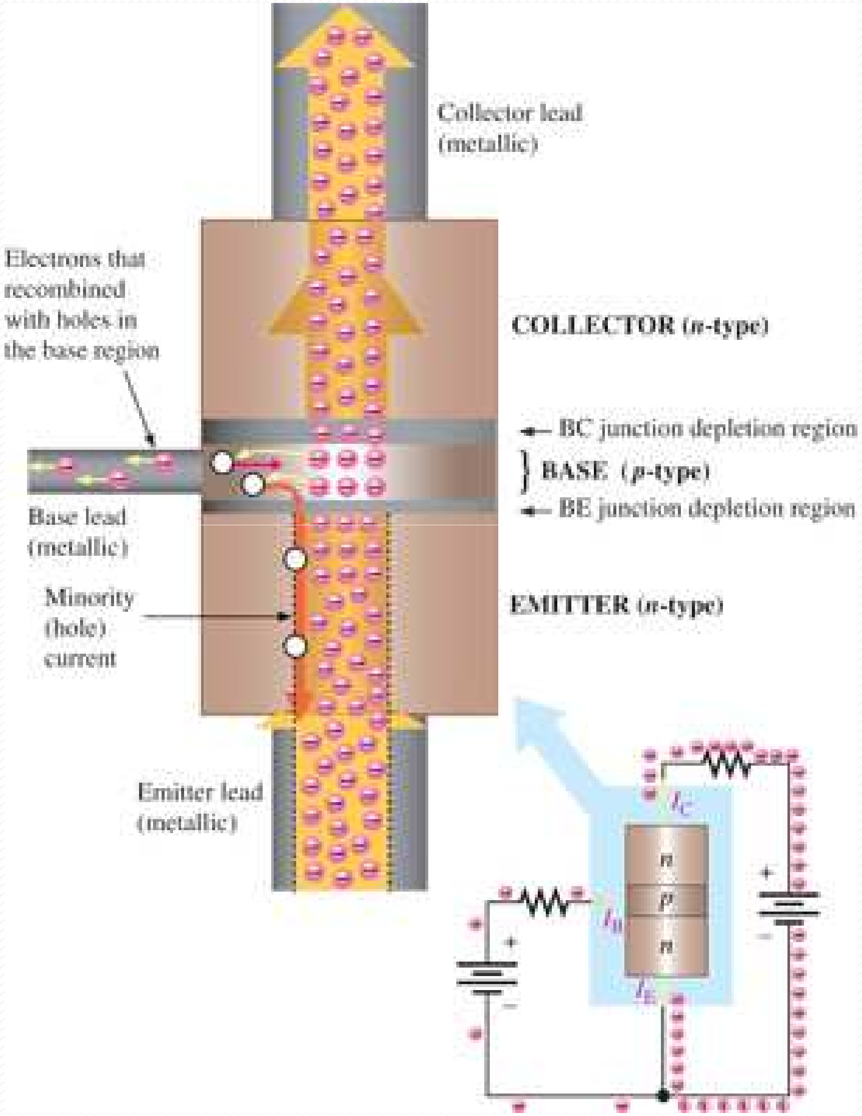

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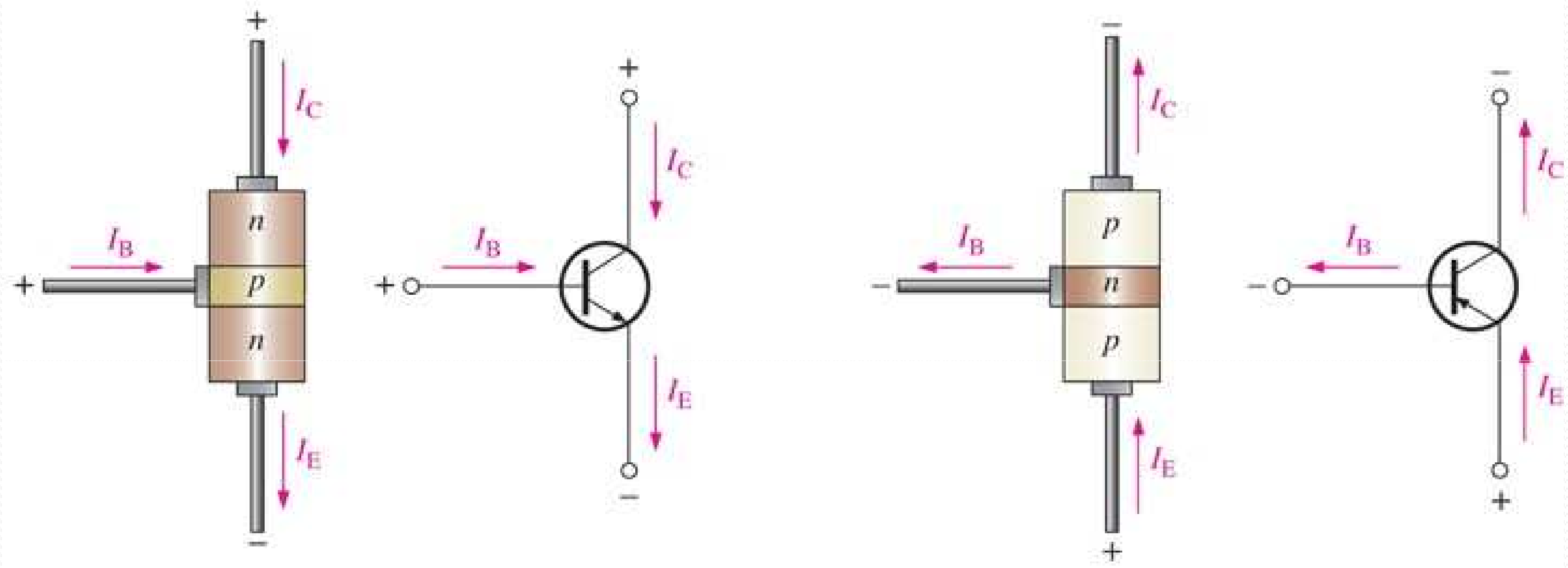
Transistor currents.



(a) *npn* (b) *pnp*

The direction of conventional current is in the direction of the arrow on the emitter terminal. The emitter current is the sum of the collector current and the small base current. That is, $I_E = I_C + I_B$.

DC Beta (βDC) and DC Alpha (αDC)

The dc current gain of a transistor is the ration of the dc collector current (*IC*) to the dc base current (*IB*) and is designated dc **beta** (βDC)

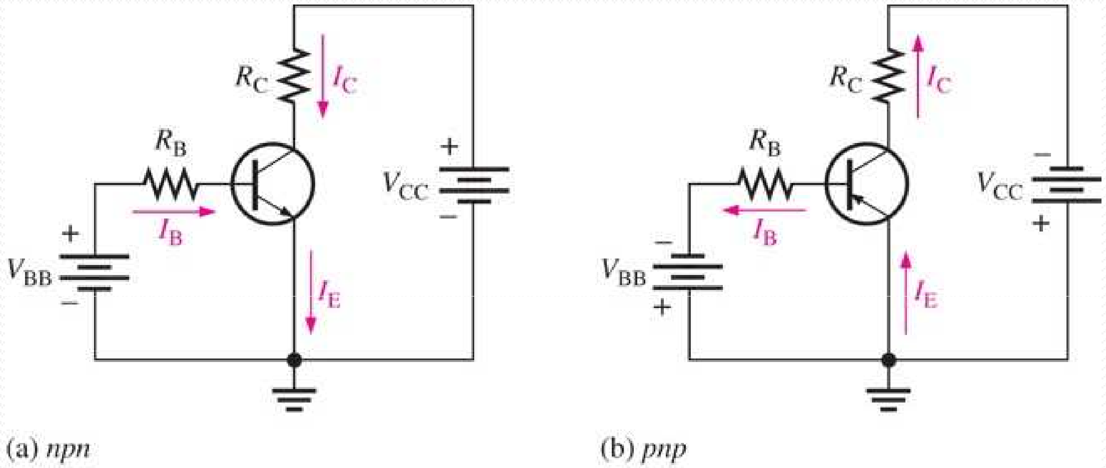
$$\beta_{DC} = h_{FE} = \frac{I_C}{I_B}$$

The ration of the dc collector current (*IC*) to the dc emitter current (*IE*) is the dc **alpha** (αDC)

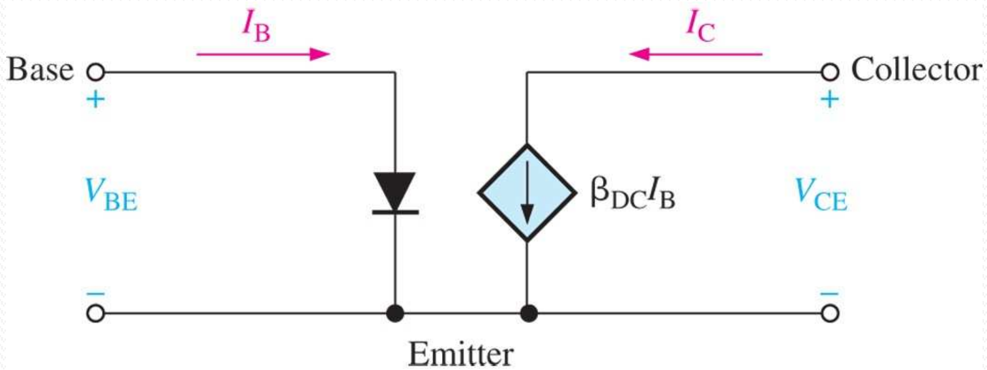
$$\alpha_{DC} = \frac{I_C}{I_E}$$

4. BJT characteristics and parameters

Transistor dc bias circuits.



Transistor DC Model



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BJT Circuit Analysis

I_B : dc base current

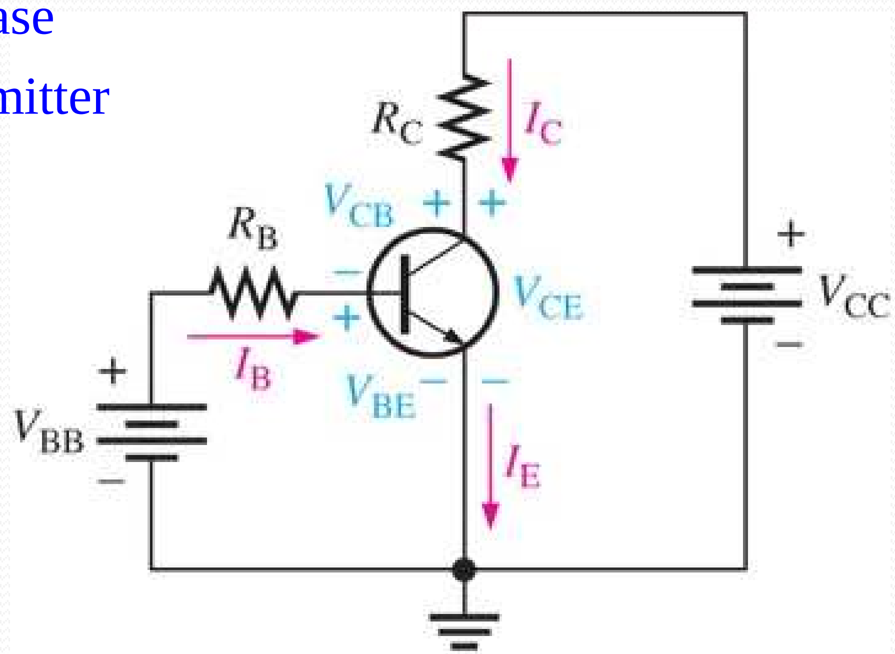
I_E : dc emitter current

I_C : dc collector current

V_{BE}: dc voltage at base with respect to emitter

V_{CB}: dc voltage at collector with respect to base

V_{CE}: dc voltage at collector with respect to emitter



$$V_{BE} \cong 0.7V$$

Since the emitter is at ground (0 V), by Kirchhoff's voltage law, the voltage across R_B is

$$V_{R_B} = V_{BB} - V_{BE}$$

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Also, by Ohm's law $V_{R_B} = I_B R_B$

Substituting for VRB yields $I_B R_B = V_{BB} - V_{BE}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

The voltage at the collector with respect to the ground emitter is

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across *RC* is

$$V_{R_C} = I_C R_C$$

The voltage at the collector with respect to the emitter can be written as

$$V_{CE} = V_{CC} - I_C R_C$$

Where $I_C = \beta_{DC} I_B$

The voltage across the reverse-biased collector –base junction is $V_{CB} = V_{CE} - V_{BE}$

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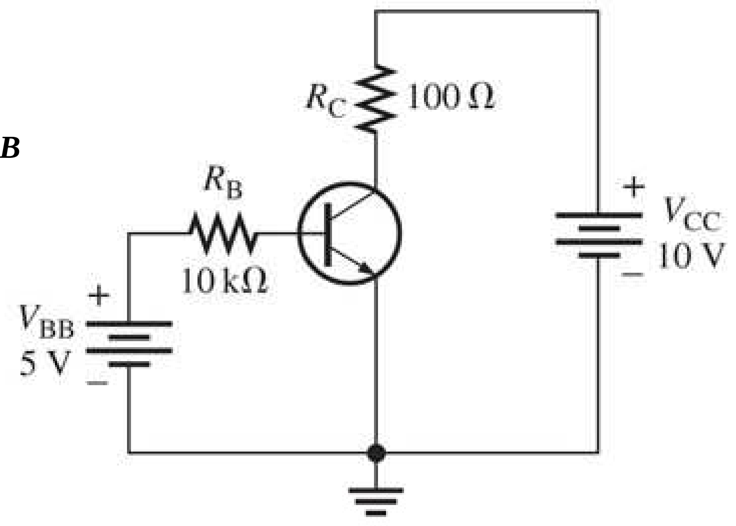
Example 1

Determine I_B, I_C I_E V_{BE}, V_{CE}, *and* V_{CB}

The transistor has a βDC = 150



Solution

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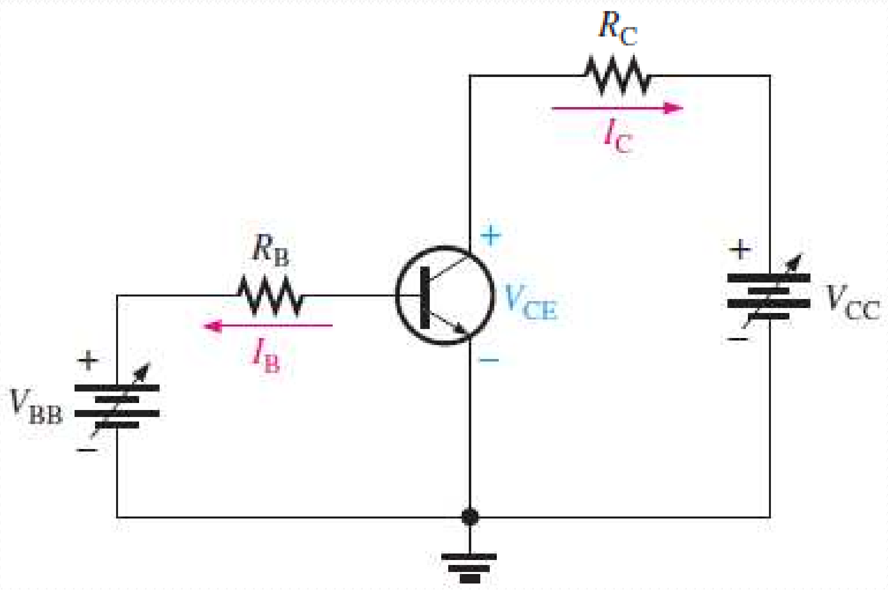
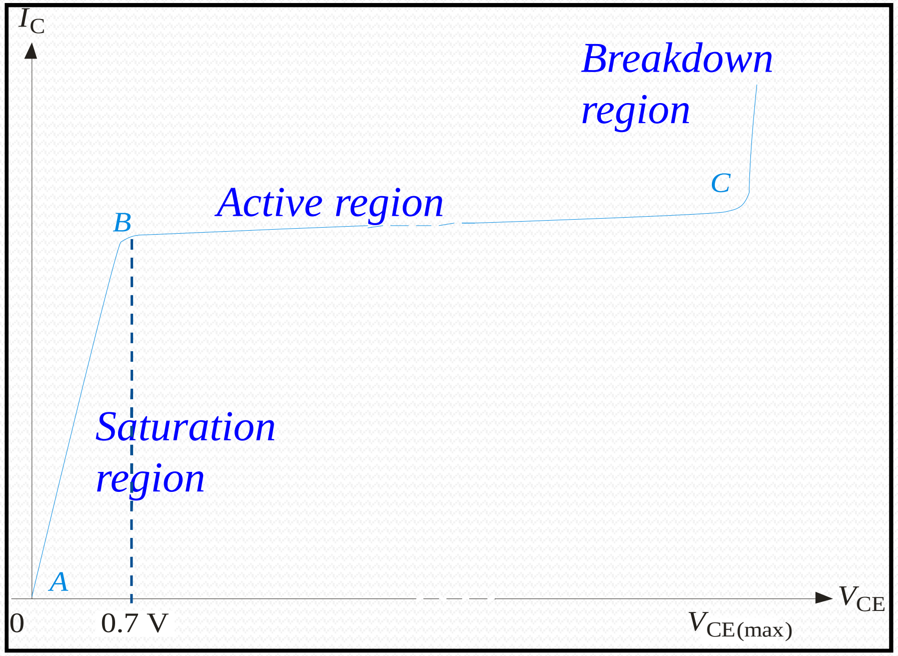
Collector Characteristic Curves

Using a circuit like that shown in Figure below , a set of *collector characteristic curves* can be generated that show how the collector current, I_C, varies with the collector-to-emitter voltage, V_{CE}, for specified values of base current, I_B. Notice in the circuit diagram that both V_{BB} and V_{CC} are variable sources of voltage.





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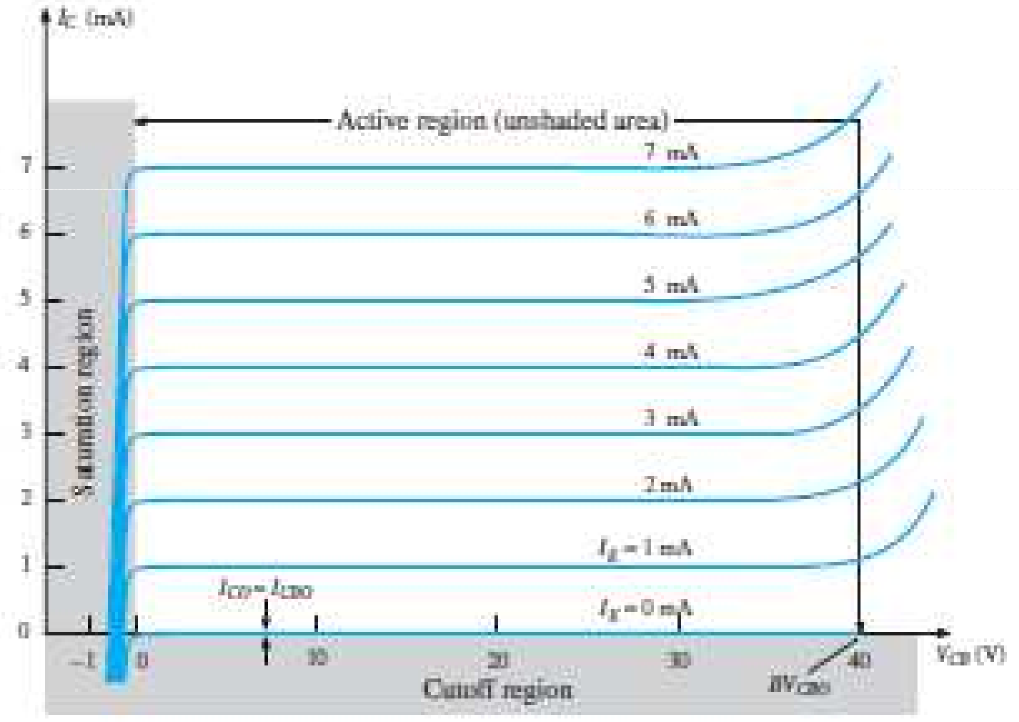
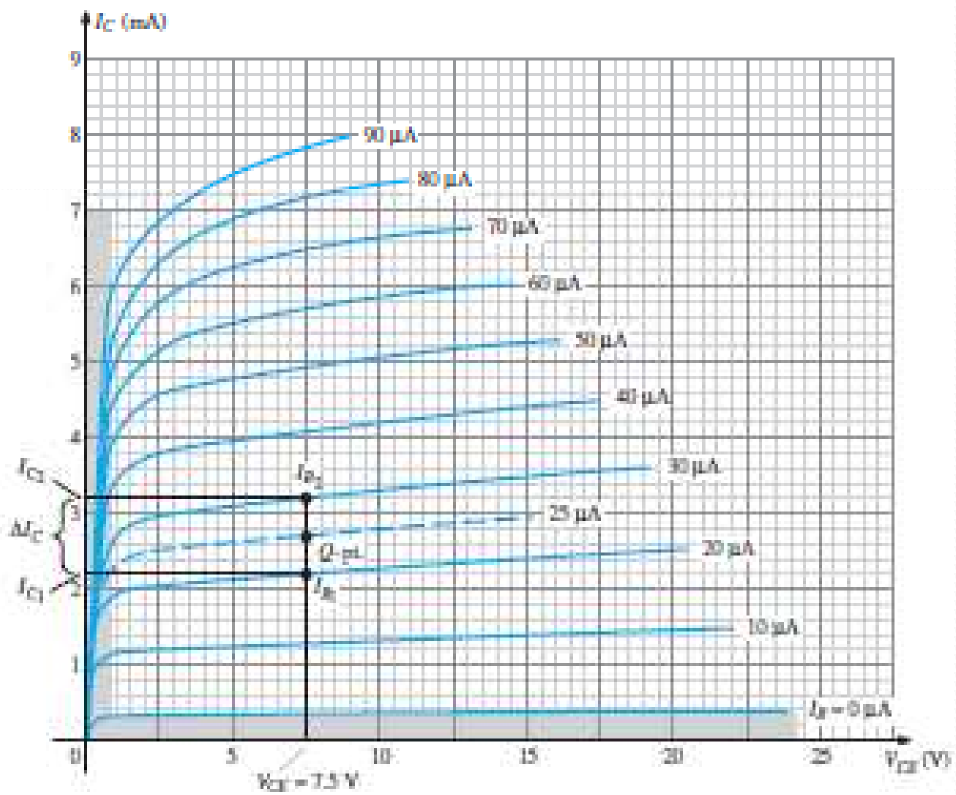
A family of collector characteristic curves is produced when I_C versus V_{CE} is plotted for several values of I_B, as illustrated in Figure below . When $I_B = 0$, the transistor is in the cutoff region although there is a very small collector leakage current as indicated. **Cutoff** is the nonconducting state of a transistor. The amount of collector leakage current for $I_B = 0$ is exaggerated on the graph for illustration.



Example 2

What is the β_{DC} for the transistor shown?

Solution



$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$
$$= \frac{3.2\text{ mA} - 2.2\text{ mA}}{30\ \mu\text{A} - 20\ \mu\text{A}} = \frac{1\text{ mA}}{10\ \mu\text{A}}$$
$$= \mathbf{100}$$

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\text{ mA}}{25\ \mu\text{A}} = \mathbf{108}$$

5. Maximum Transistor Ratings

A BJT, like any other electronic device, has limitations on its operation. These limitations are stated in the form of maximum ratings and are normally specified on the manufacturer's datasheet. Typically, maximum ratings are given for collector-to-base voltage, collector-to-emitter voltage, emitter-to-base voltage, collector current, and power dissipation.

The product of V_{CE} and I_C must not exceed the maximum power dissipation. Both V_{CE} and I_C cannot be maximum at the same time. If V_{CE} is maximum, I_C can be calculated as

$$I_C = \frac{P_{D(max)}}{V_{CE}}$$

If I_C is maximum, V_{CE} can be calculated by rearranging the previous equation as follows:

$$V_{CE} = \frac{P_{D(max)}}{I_C}$$

For the device of below Fig. the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{max}} = V_{CE} I_C = 300 \text{ mW}$$

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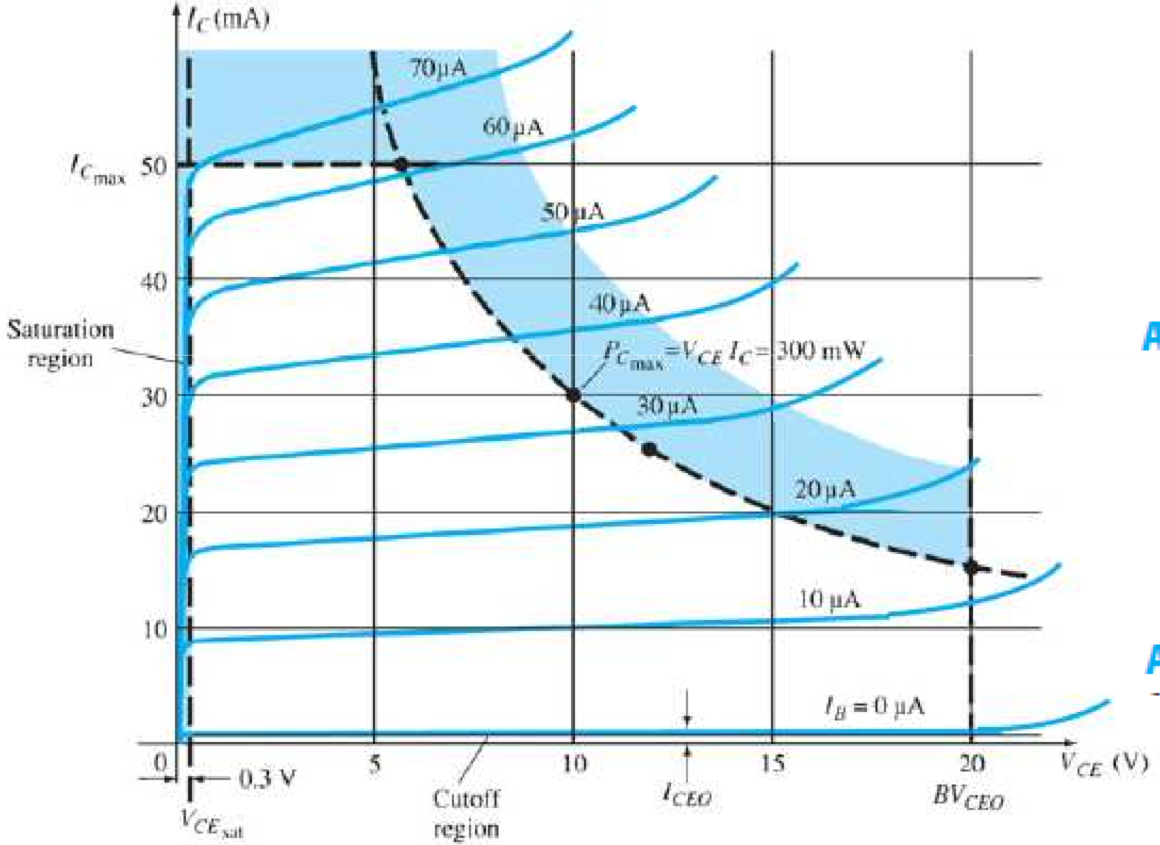


At $I_{C_{max}}$

$$V_{CE} I_C = 300 \text{ mW}$$
$$V_{CE}(50 \text{ mA}) = 300 \text{ mW}$$
$$V_{CE} = \frac{300 \text{ mW}}{50 \text{ mA}} = 6 \text{ V}$$

At $V_{CE_{max}}$

$$(20 \text{ V}) I_C = 300 \text{ mW}$$
$$I_C = \frac{300 \text{ mW}}{20 \text{ V}} = 15 \text{ mA}$$

At $I_C = \frac{1}{2} I_{C_{max}}$

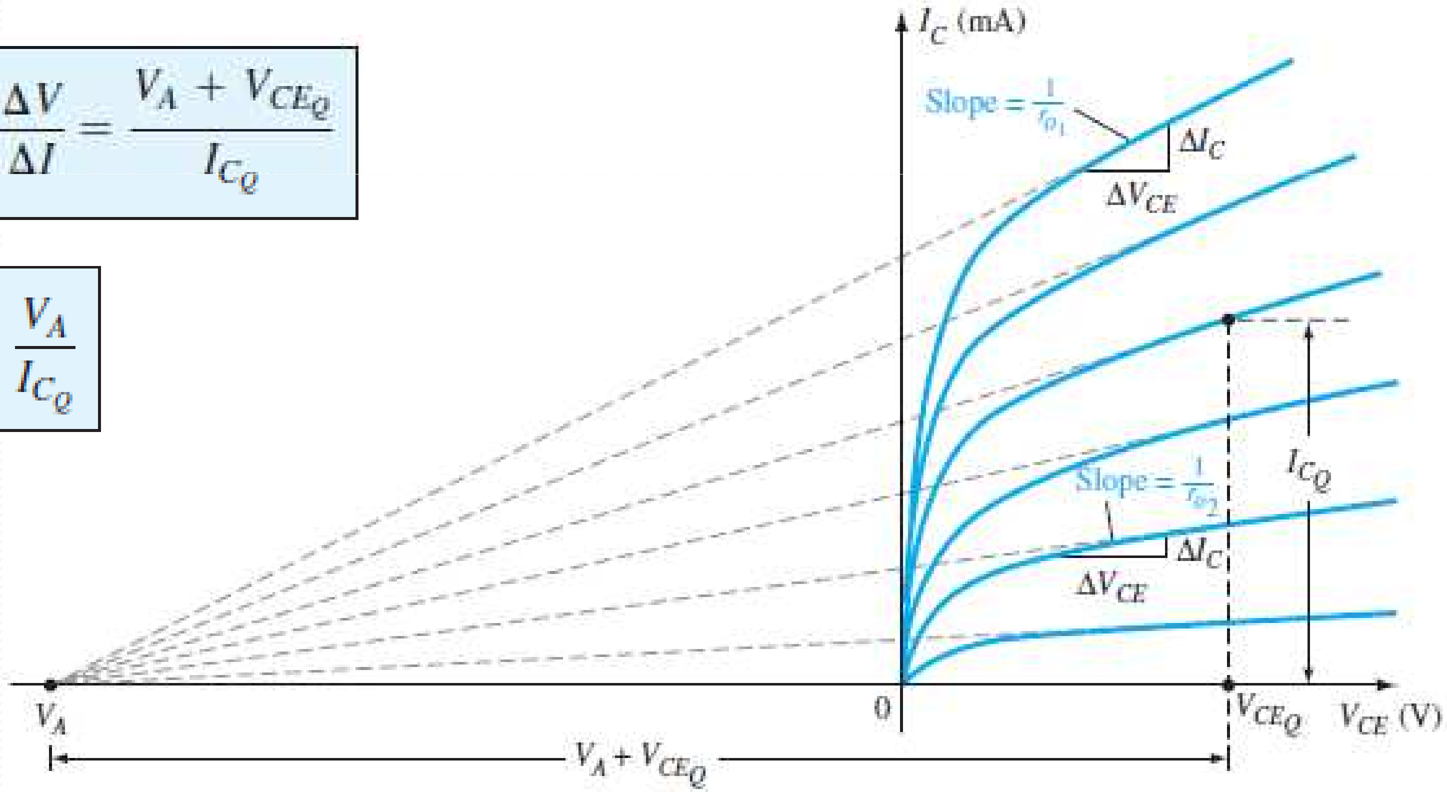
$$V_{CE}(25 \text{ mA}) = 300 \text{ mW}$$
$$V_{CE} = \frac{300 \text{ mW}}{25 \text{ mA}} = 12 \text{ V}$$

Early Voltage

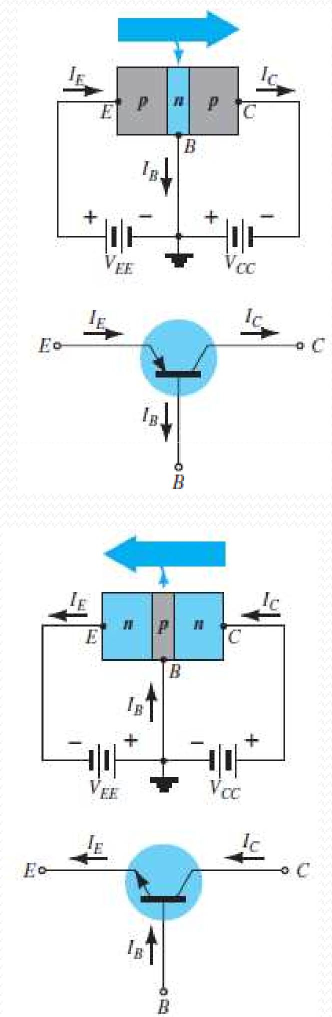
Early in 1952. As the base current increases the slope of the line increases, resulting in an increase in output impedance with increase in base and collector current. For a particular collector and base current as shown in Fig. 5.15, the output impedance can be found using the following equation:

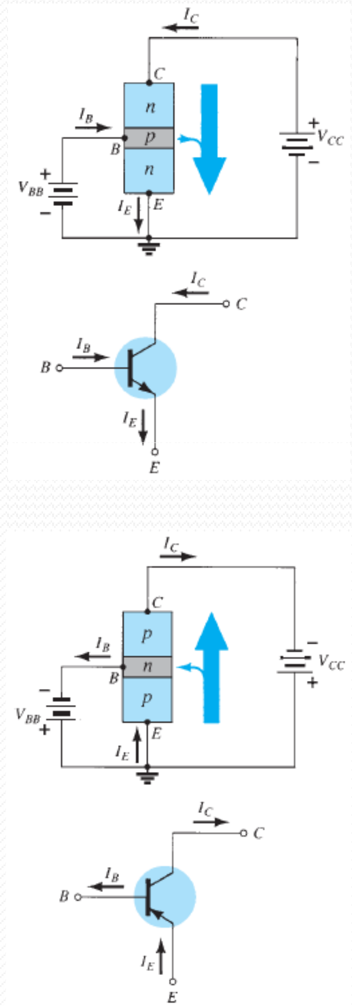
$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}$$

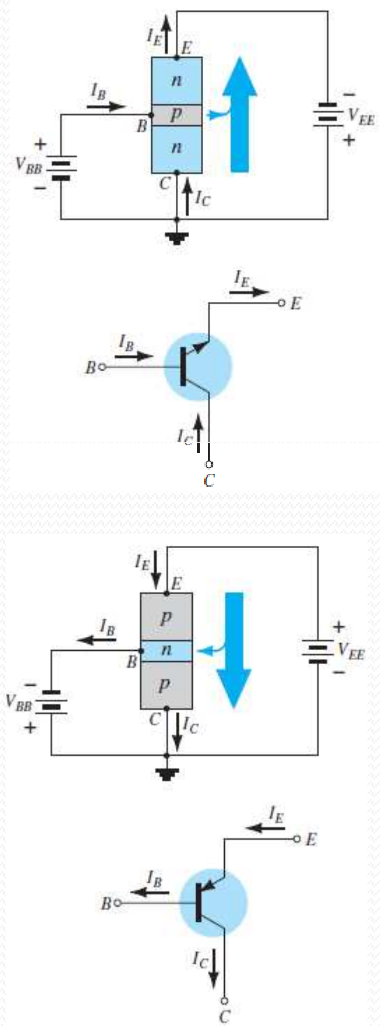
$$r_o \cong \frac{V_A}{I_{C_Q}}$$



6. Common Circuit Configuration







Common base configuration | Common emitter configuration | Common collector configuration

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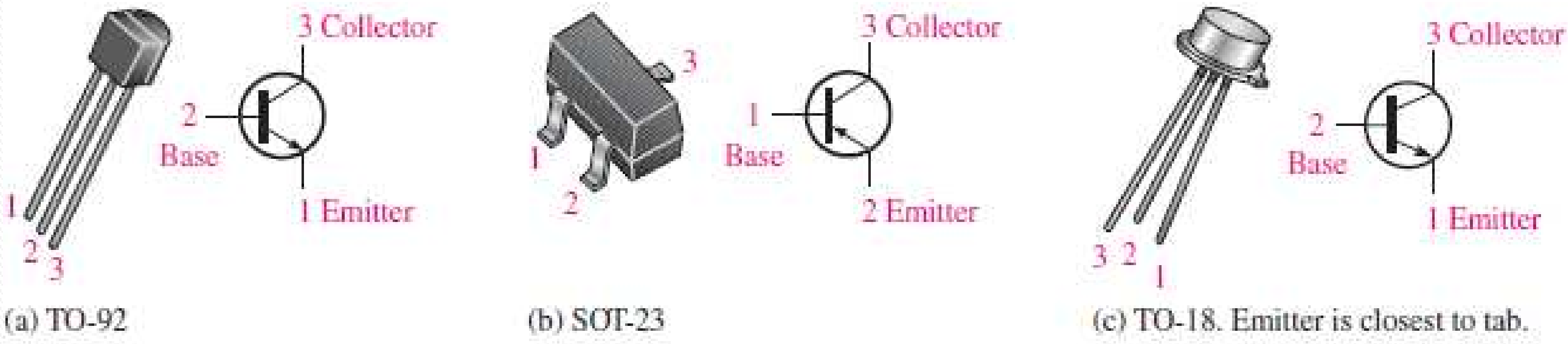
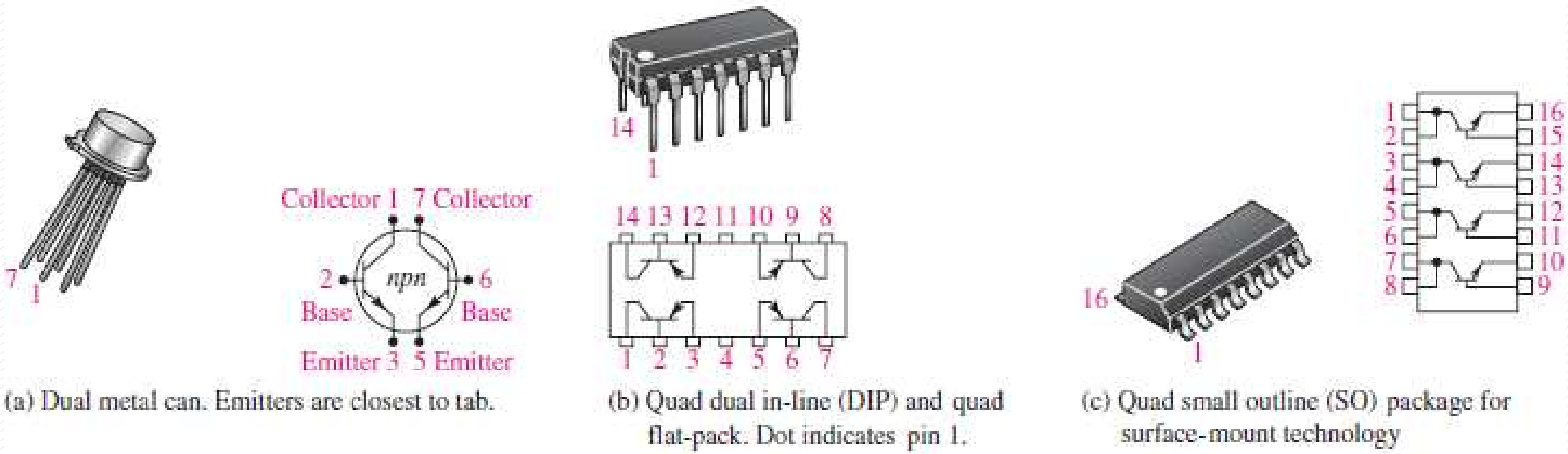
7. Transistor Categories and Packaging



Plastic and metal cases for general-purpose/small-signal transistors. Pin configurations may vary. Always check the datasheet (*http://fairchildsemiconductor.com/*).



Examples of multiple-transistor packages.

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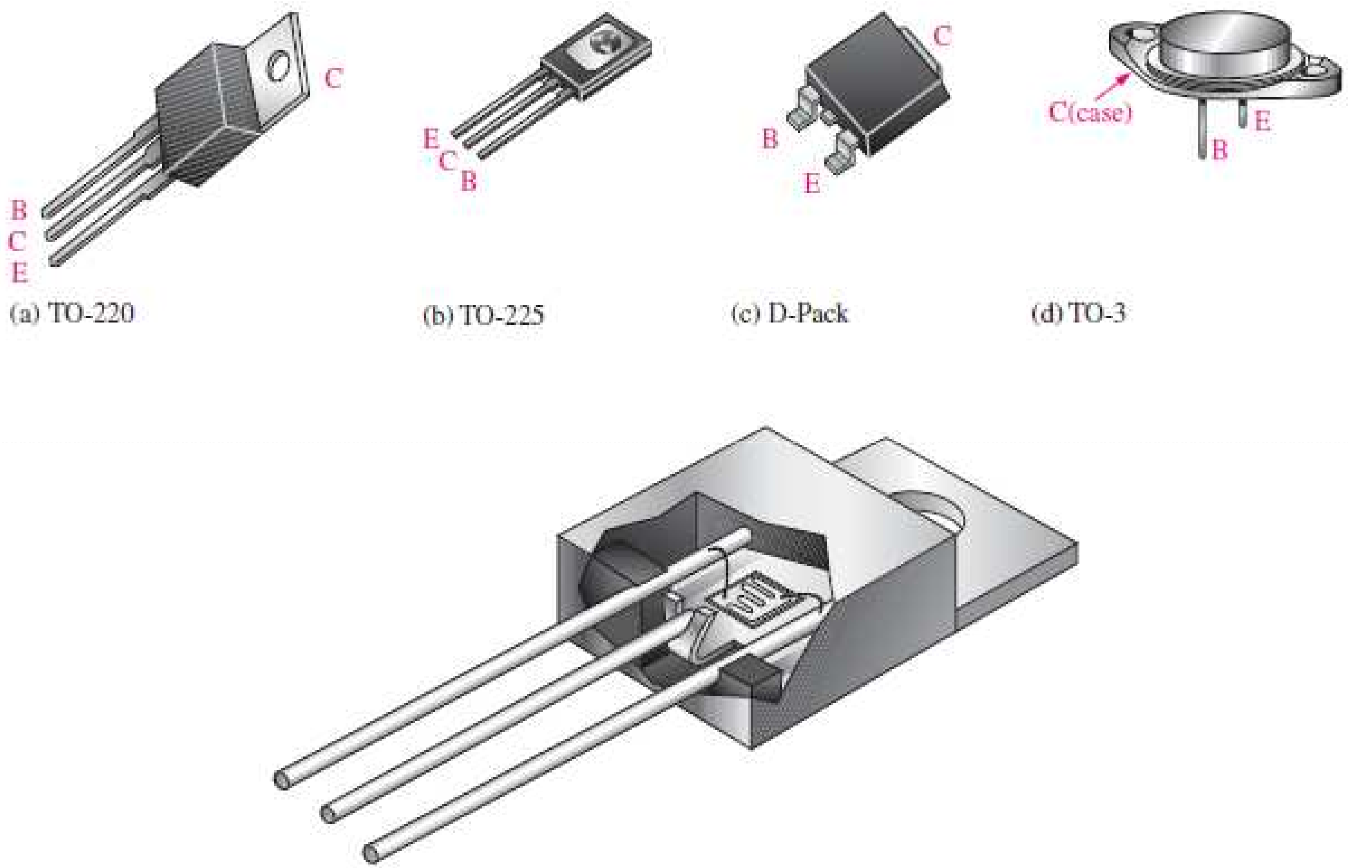


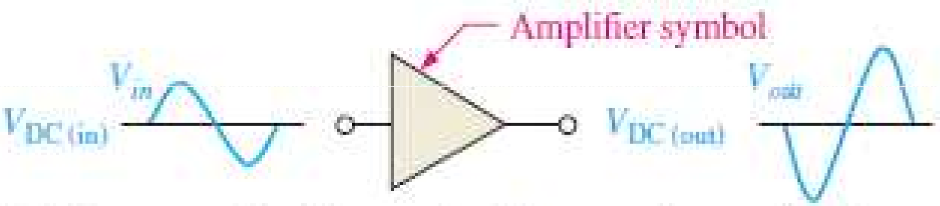
(e) Greatly enlarged cutaway view of tiny transistor chip mounted in the encapsulated package

Examples of power transistors and packages.

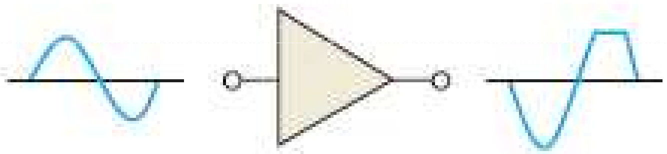
8. The DC Operating Point

DC Bias

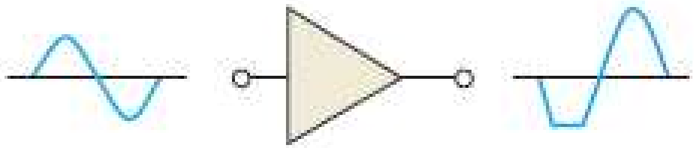
Bias establishes the dc operating point (**Q-point**) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied.



(a) Linear operation: larger output has same shape as input except that it is inverted



(b) Nonlinear operation: output voltage limited (clipped) by cutoff

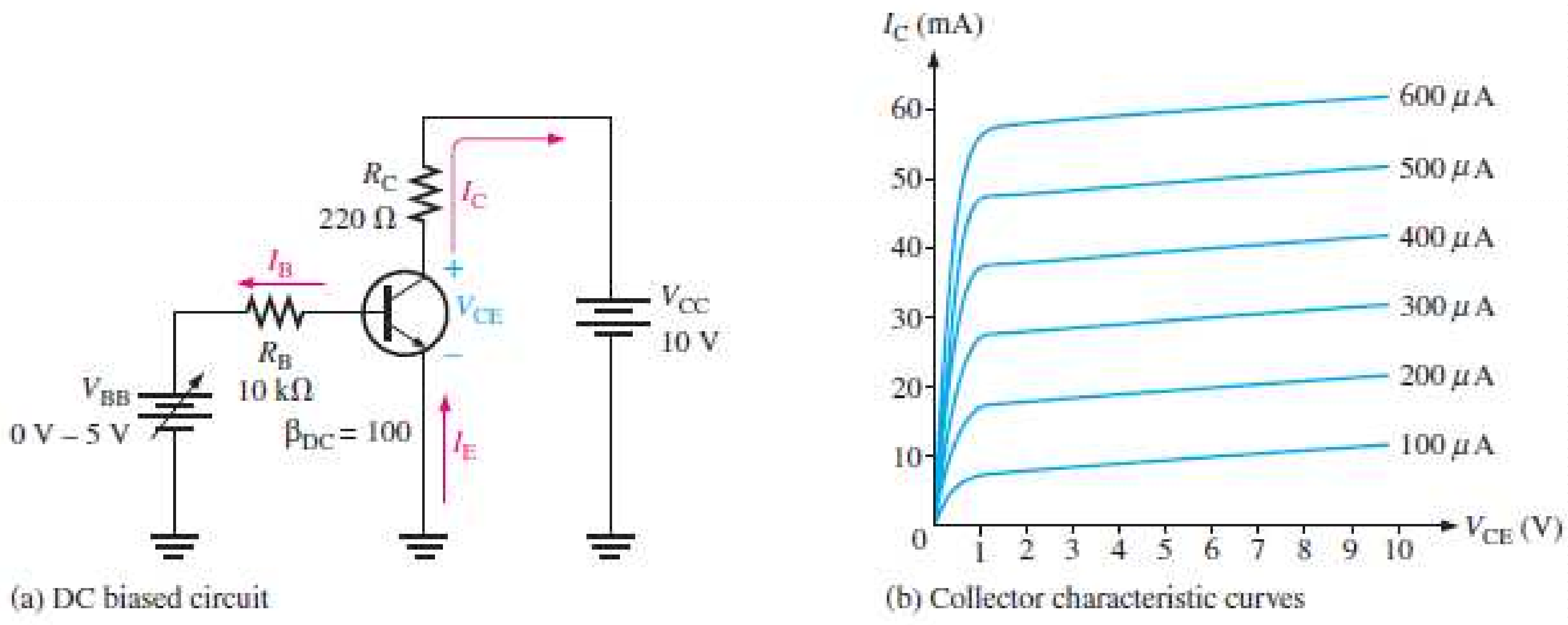


(c) Nonlinear operation: output voltage limited (clipped) by saturation

Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Bipolar Junction Transistor

Graphical Analysis The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.

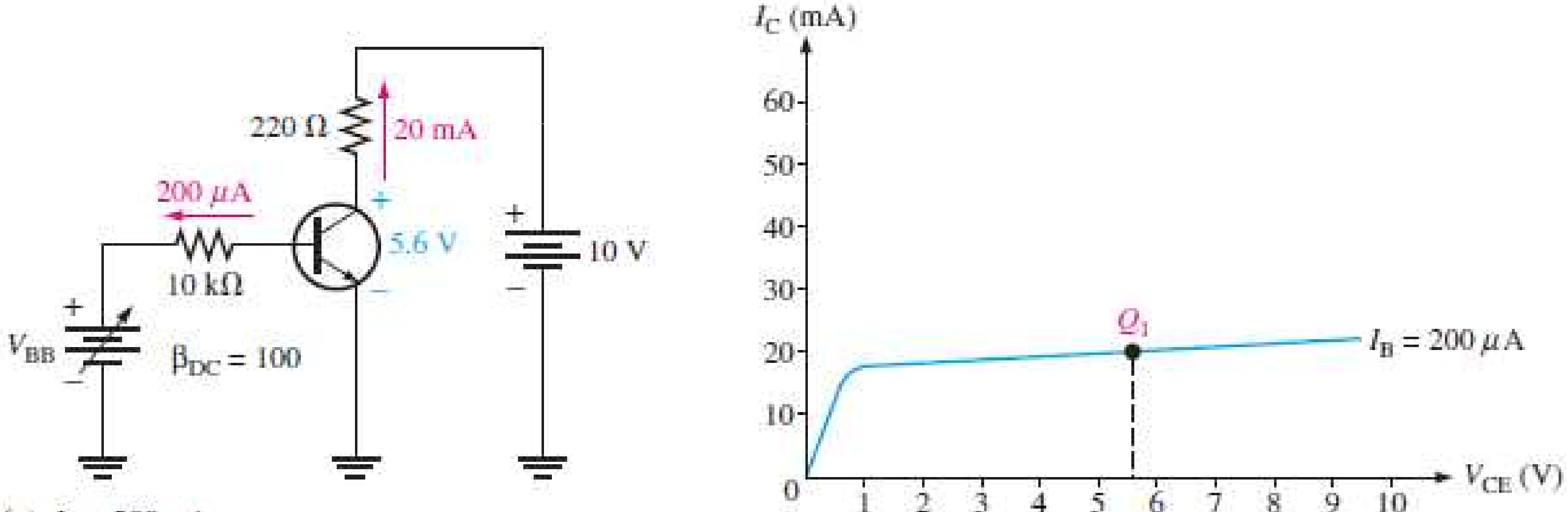


▲ FIGURE 5–2

Bipolar Junction Transistor

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$



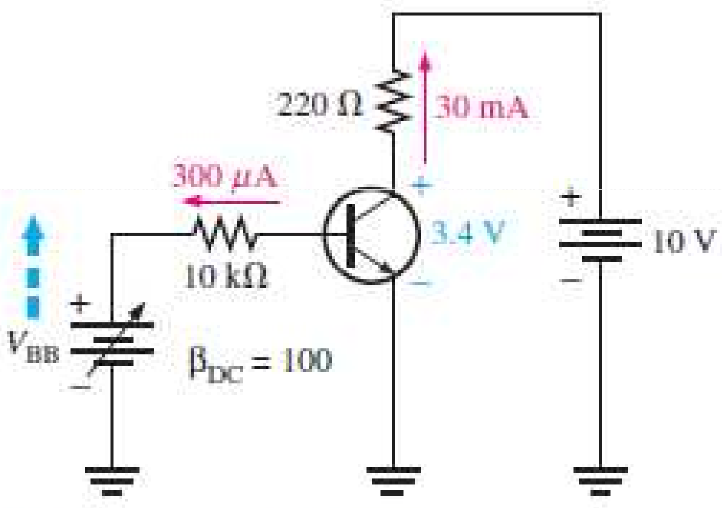
(a) $I_B = 200\ \mu$A

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

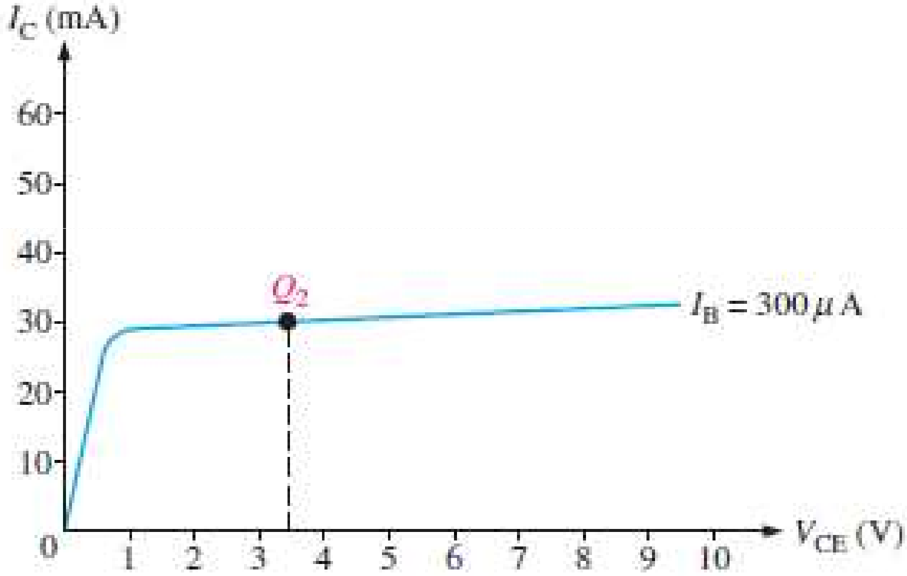
Bipolar Junction Transistor

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$



(b) Increase I_B to 300 μA by increasing V_{BB}



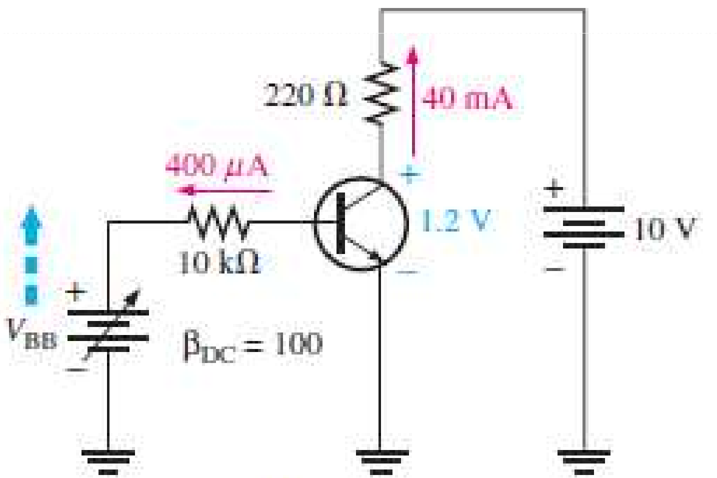
The Q-point for this condition is indicated by Q_2 on the graph.

Bipolar Junction Transistor

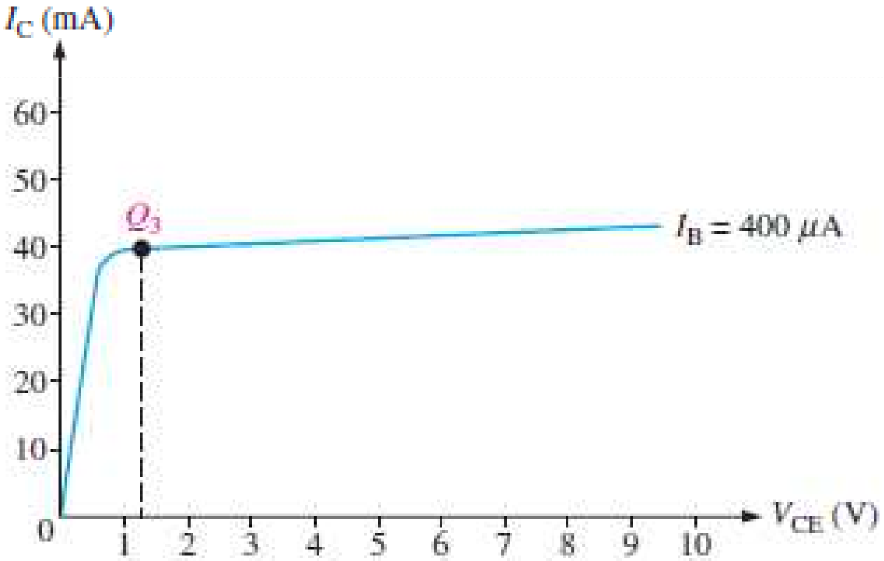
Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

Q_3 is the corresponding Q-point on the graph.



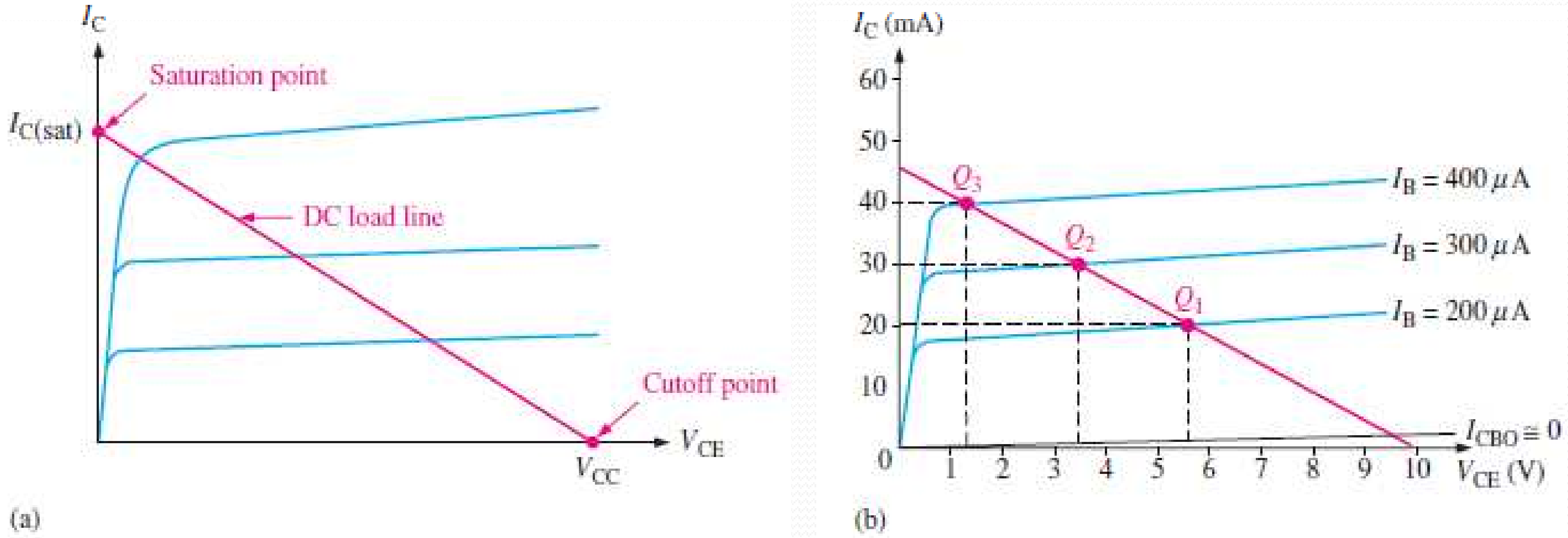
(c) Increase I_B to 400 μA by increasing V_{BB}



Bipolar Junction Transistor

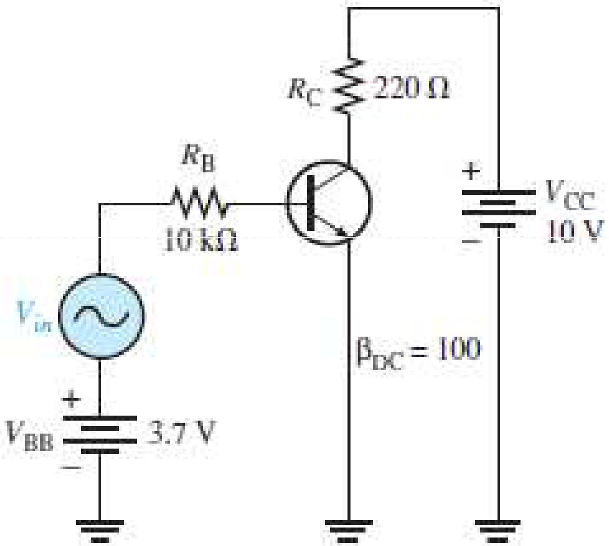
DC Load Line The dc operation of a transistor circuit can be described graphically using a **dc load line**. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where $V_{CE} = V_{CC}$ on the x-axis, as shown in Figure 5–4(a). The load line is determined by the external circuit (V_{CC} and R_C), not the transistor itself, which is described by the characteristic curves. the equation for I_C is

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$



▲ FIGURE 5–4

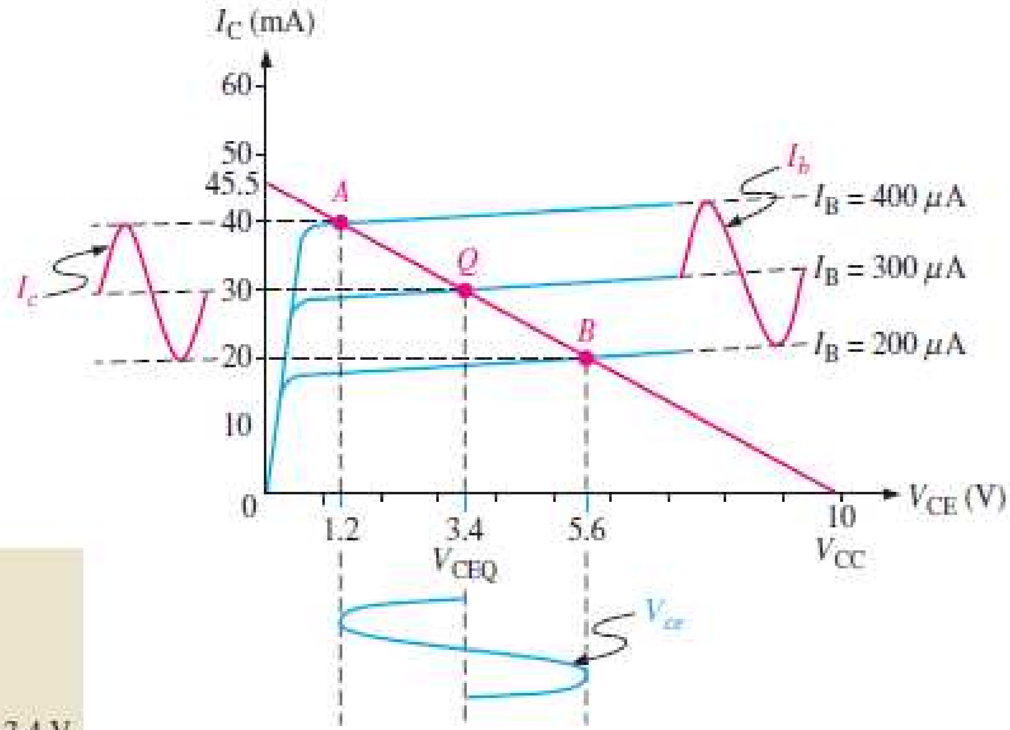
Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

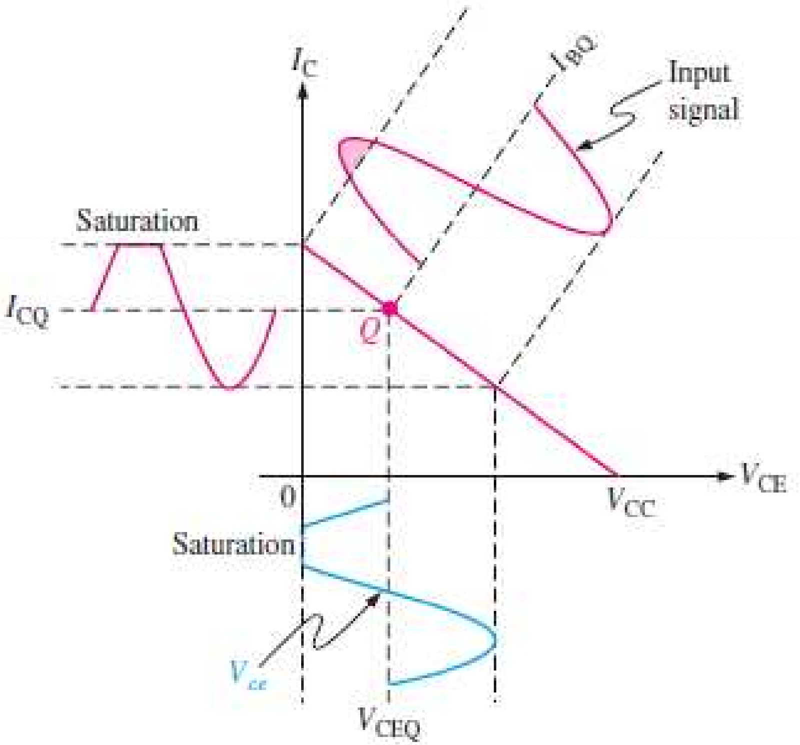
$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$



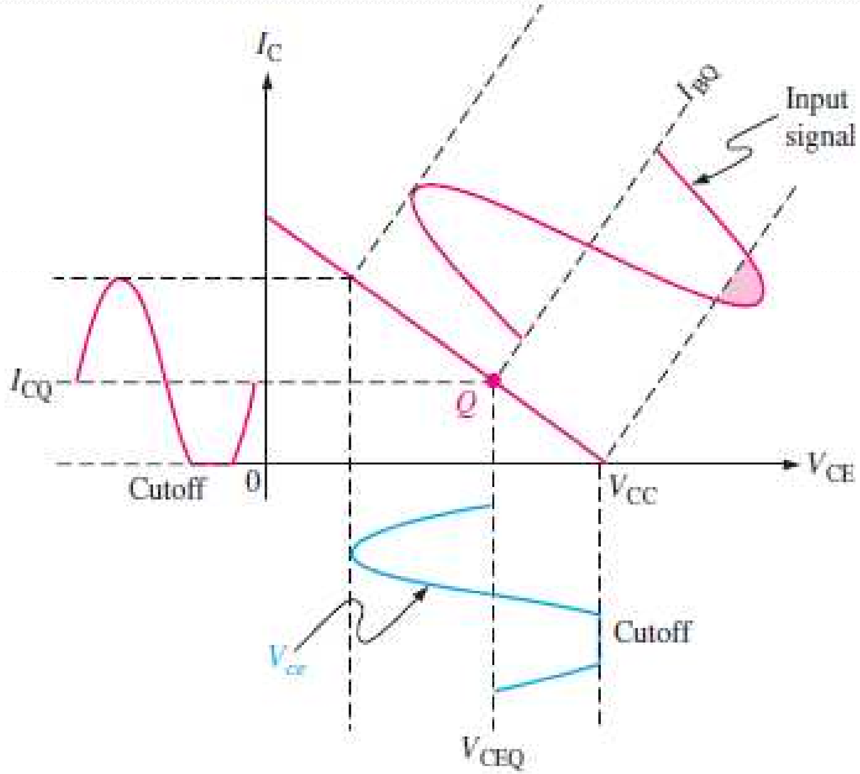
▲ FIGURE 5–5

Bipolar Junction Transistor

Waveform Distortion As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the V_{ce} waveform to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6.

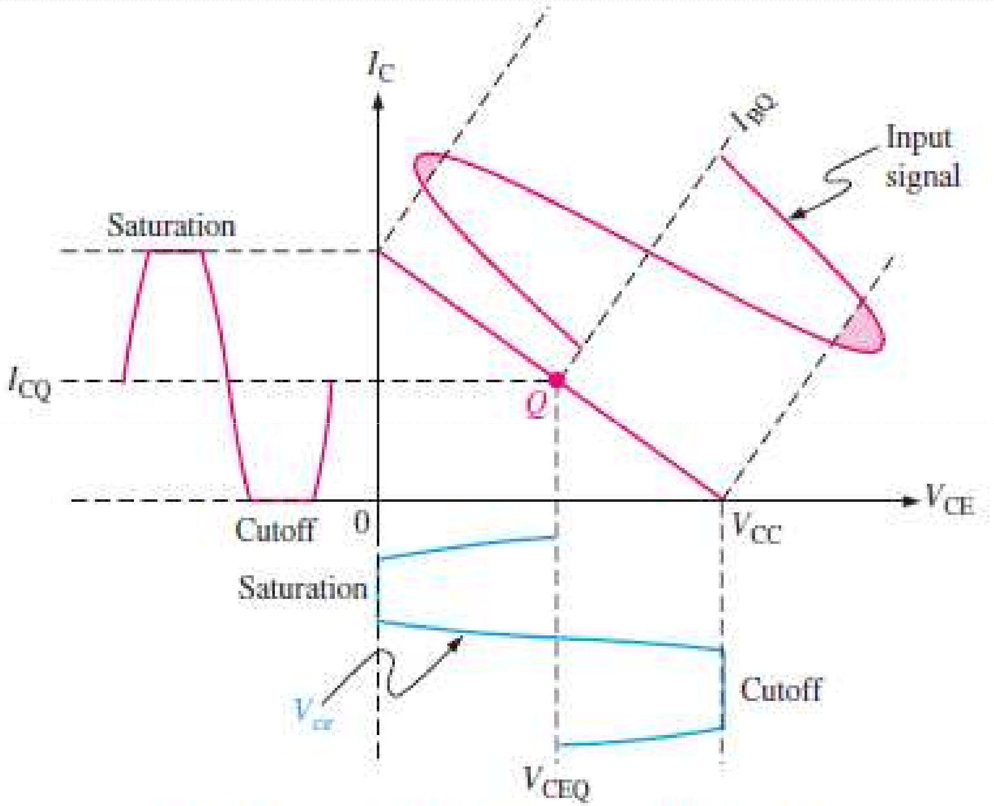


(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

Bipolar Junction Transistor

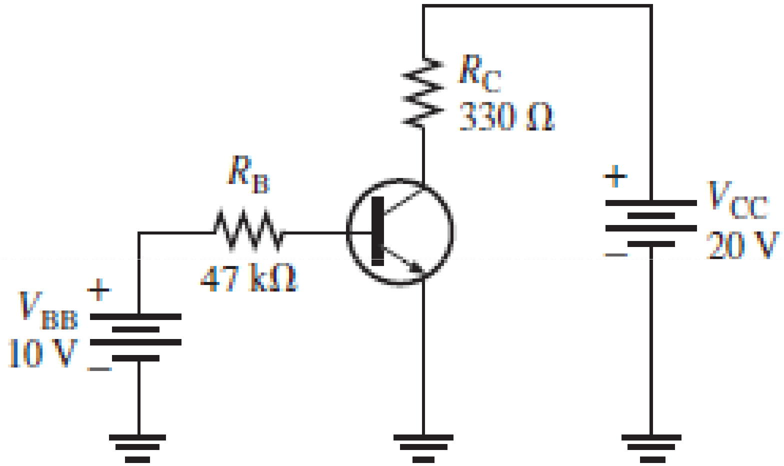


(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

▲ FIGURE 5–6

Example 3

Determine the Q-point for the circuit in below Fig. and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.



Solution

Bipolar Junction Transistor

9. Transistor Bias Circuits

9.1. voltage Divider Bias

You will now study a method of biasing a transistor for linear operation using a single-source resistive voltage divider. This is the most widely used biasing method.

To analyze a voltage-divider circuit in which I_B is small compared to I_2,

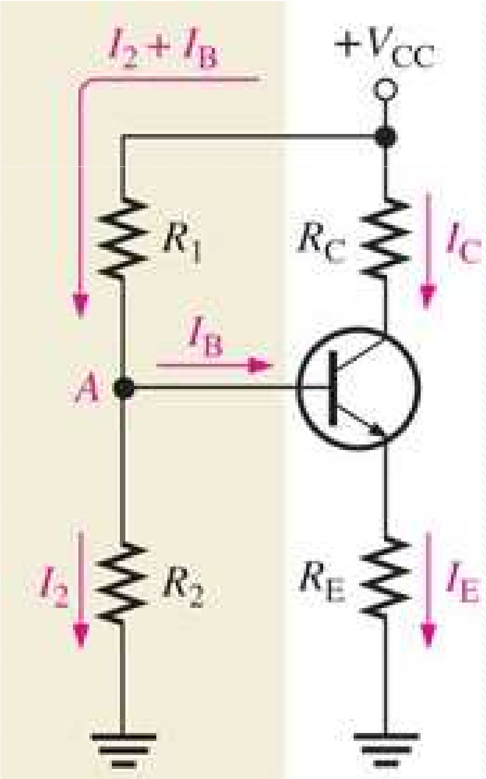
$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

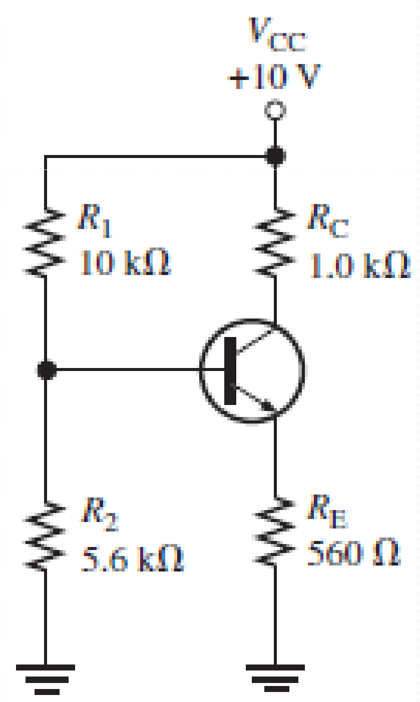


Bipolar Junction Transistor

Example 4

Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of below Fig. if $\beta_{DC} = 100$.

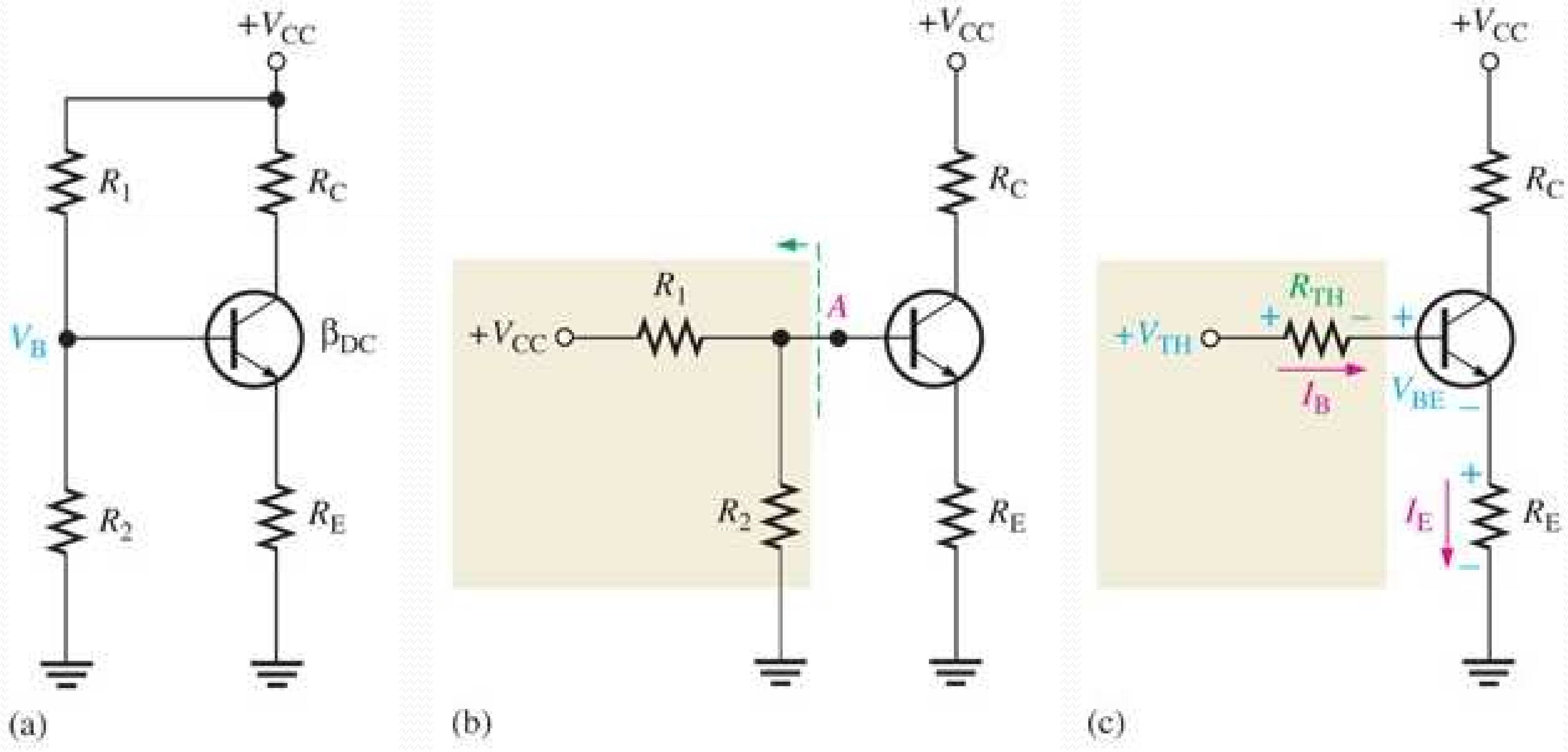
Solution



Bipolar Junction Transistor

Thevenin's Theorem Applied to Voltage-Divider Bias

To analyze a voltage-divider biased transistor circuit for base current loading effects, we will apply Thevenin's theorem to evaluate the circuit.



Bipolar Junction Transistor

The voltage at point A with respect to ground is

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

and the resistance is

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2}$$

Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

Substituting, using Ohm's law, and solving for V_{TH},

$$V_{TH} = I_BR_{TH} + V_{BE} + I_ER_E$$

Substituting I_E/β_{DC} for I_B,

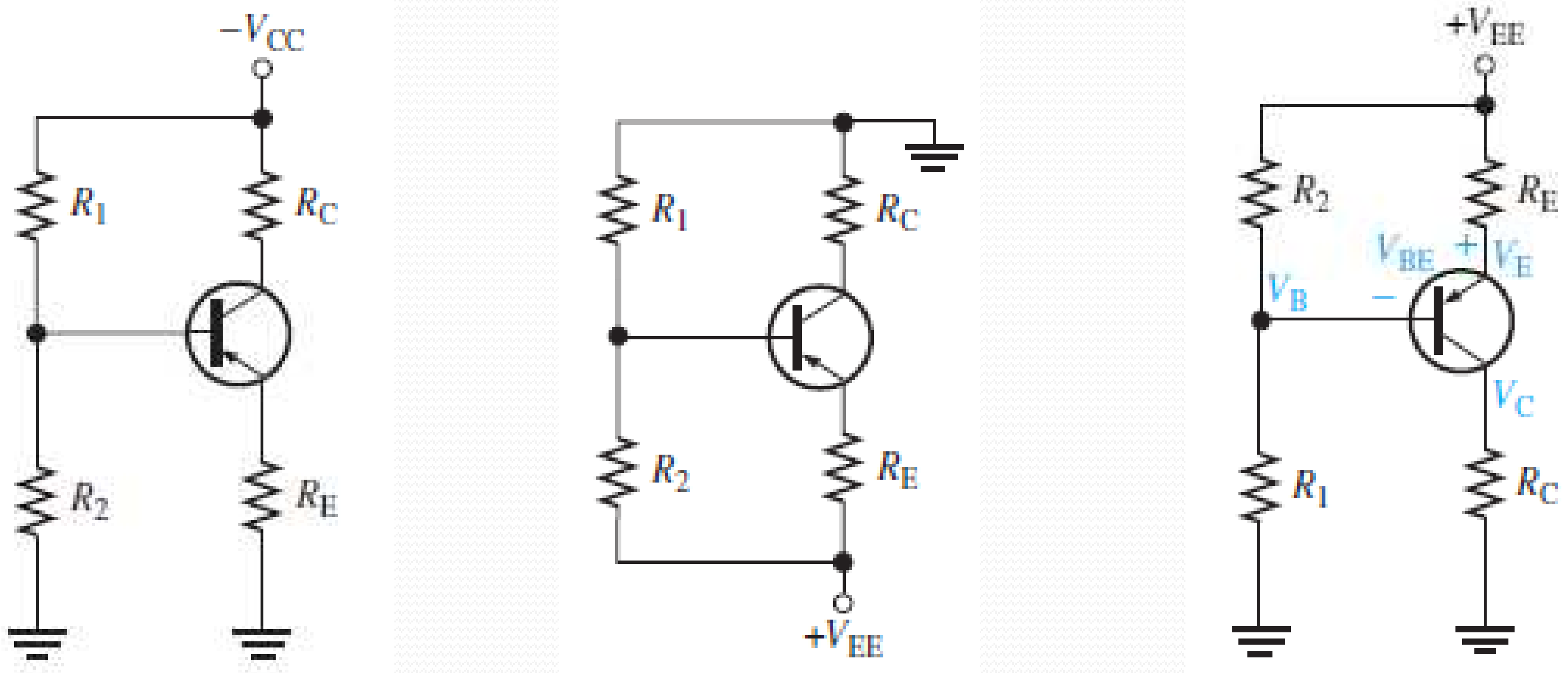
$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E,

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Bipolar Junction Transistor

Voltage-Divider Biased PNP Transistor As you know, a *pnp* transistor requires bias polarities opposite to the *npn*. This can be accomplished with a negative collector supply voltage, as in Figure 5–14(a), or with a positive emitter supply voltage, as in Figure 5–14(b).



(a) Negative collector supply voltage, V_{CC}

(b) Positive emitter supply voltage, V_{EE}

(c) The circuit in (b) redrawn

FIGURE 5–14

Bipolar Junction Transistor

The analysis procedure is the same as for an *npn* transistor circuit using Thevenin's theorem and Kirchhoff's voltage law, applying Kirchhoff's voltage law around the base-emitter circuit gives

$$V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E = 0$$

By Thevenin's theorem,

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

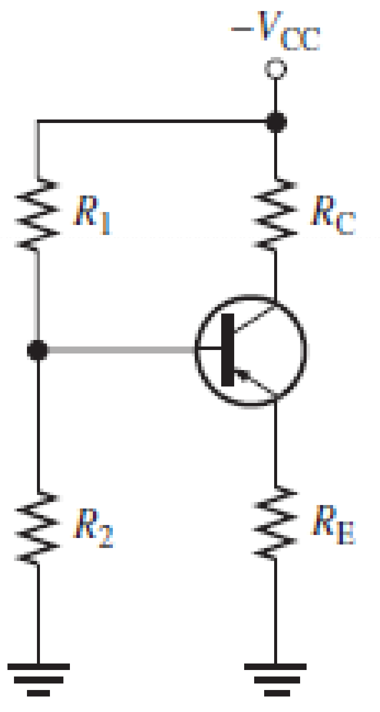
$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

The base current is

$$I_B = \frac{I_E}{\beta_{DC}}$$

The equation for I_E is

$$I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

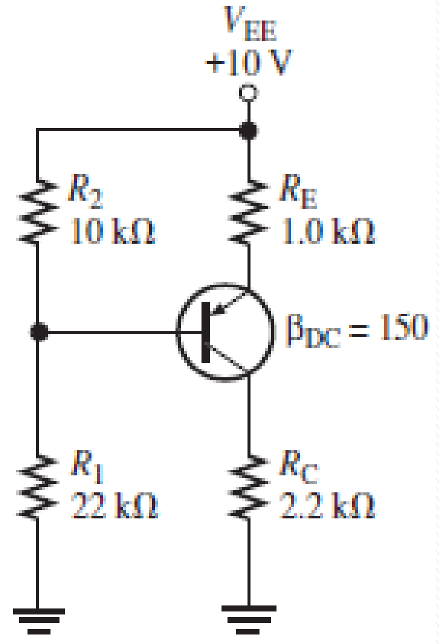


Bipolar Junction Transistor

Example 5

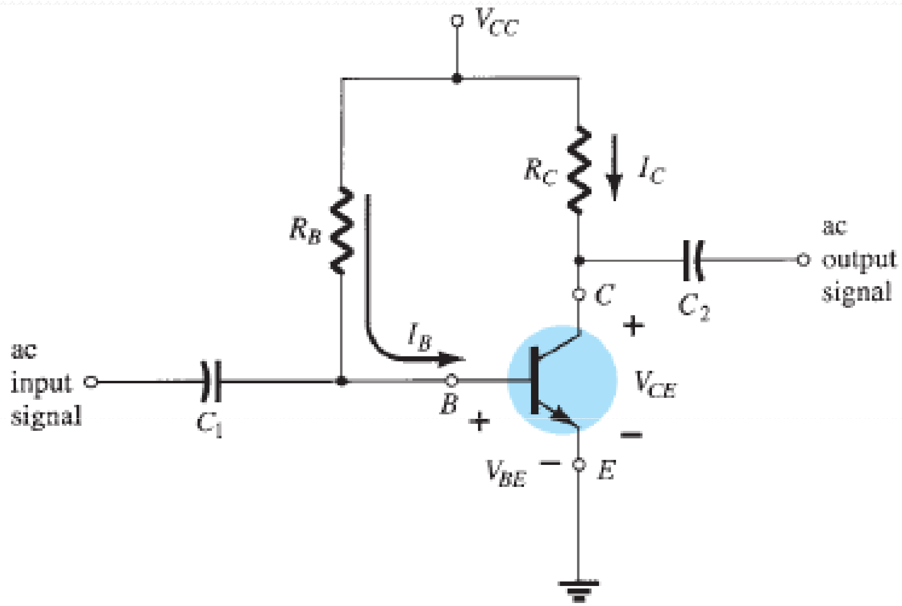
Find I_C and V_{EC} for the *pnp* transistor circuit

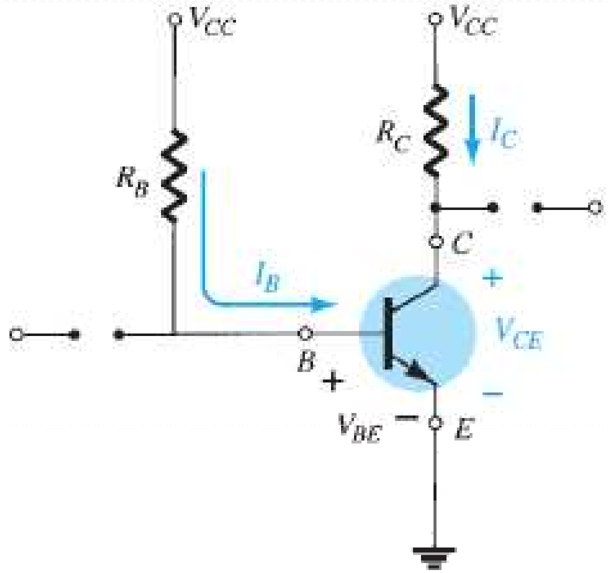
Solution



Bipolar Junction Transistor

9.2. Fixed Bias Configuration





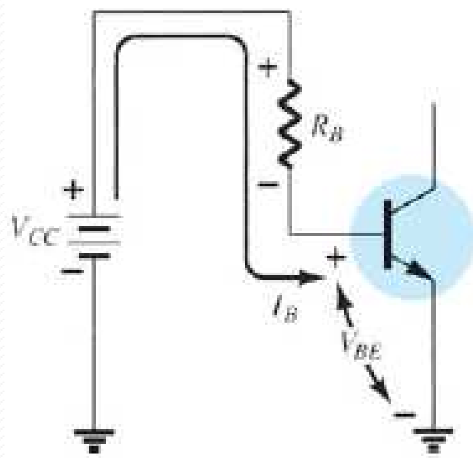
Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

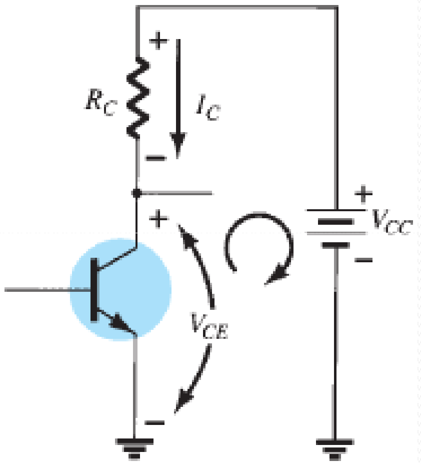
$$I_C = \beta I_B$$



Bipolar Junction Transistor

Collector–Emitter Loop

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop

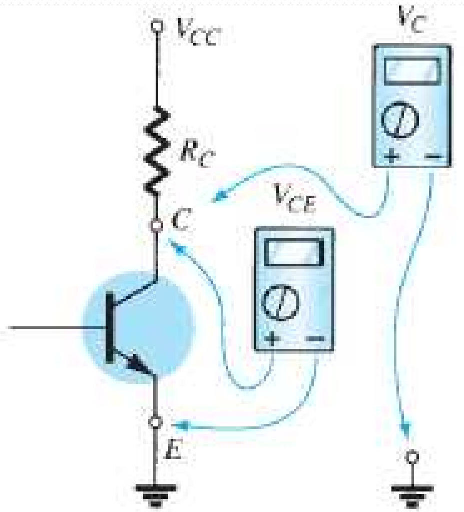


$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E \qquad V_E = 0\text{ V}$$

$$V_{CE} = V_C$$



$$V_{BE} = V_B - V_E$$

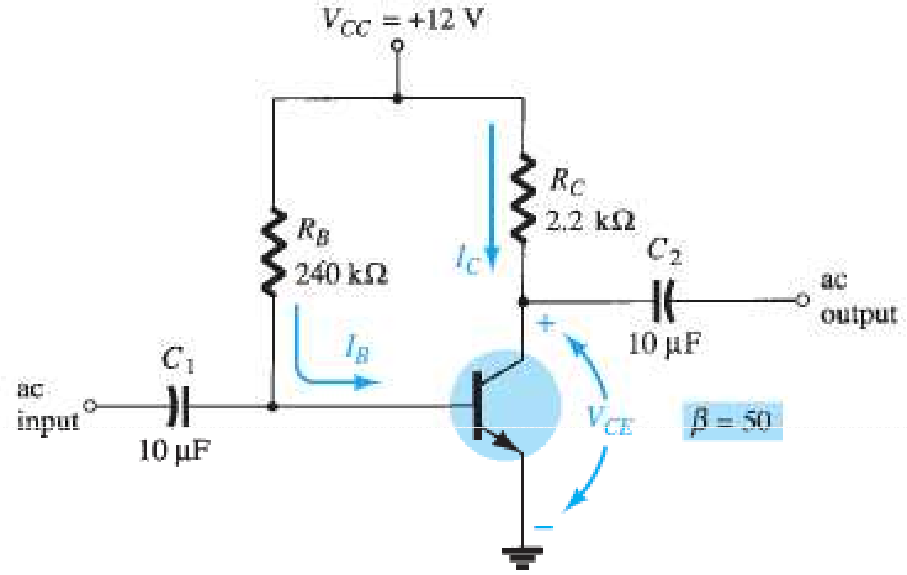
and $V_E = 0$ V, then

$$V_{BE} = V_B$$

Example 6

For the following circuit, determine

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

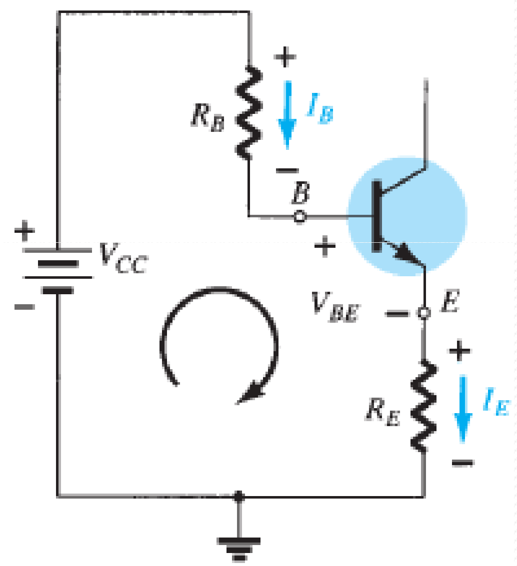


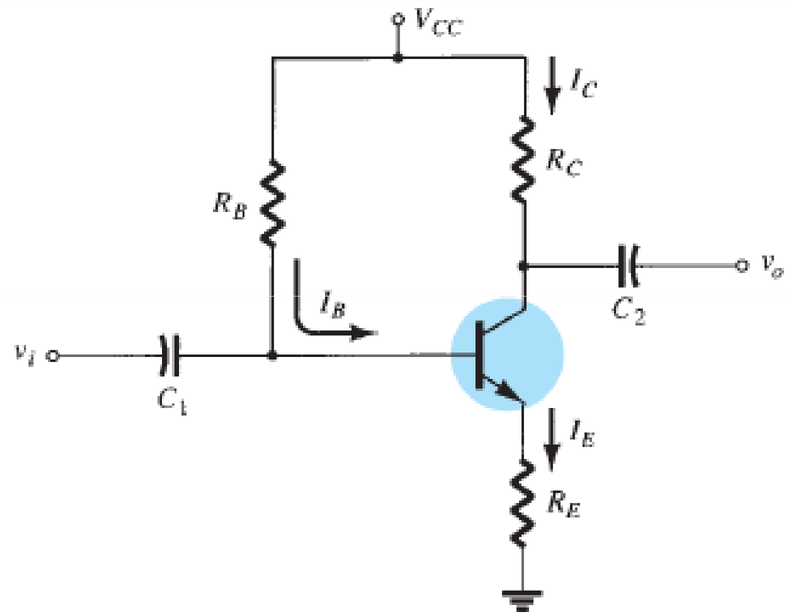
Solution

9.3. Emitter Bias Configuration

Emitter bias provides excellent bias stability in spite of changes in β or temperature.

Base–Emitter Loop





Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

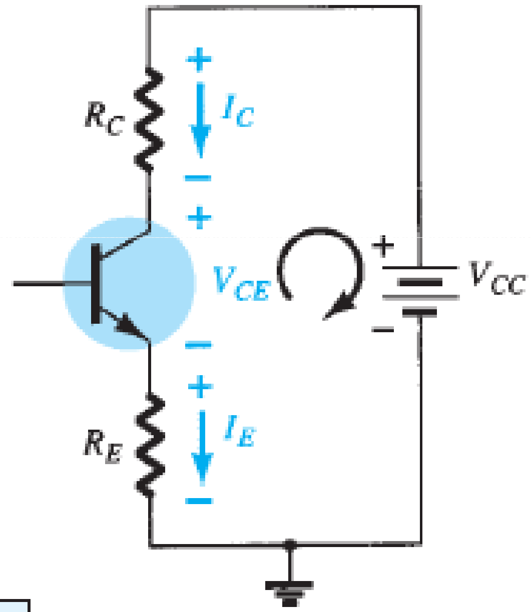
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad I_E = (\beta + 1)I_B$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0$$

Bipolar Junction Transistor

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



Collector–Emitter Loop

Writing Kirchhoff's voltage law for the indicated loop results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_E = I_E R_E$$

$$V_B = V_{CC} - I_B R_B$$

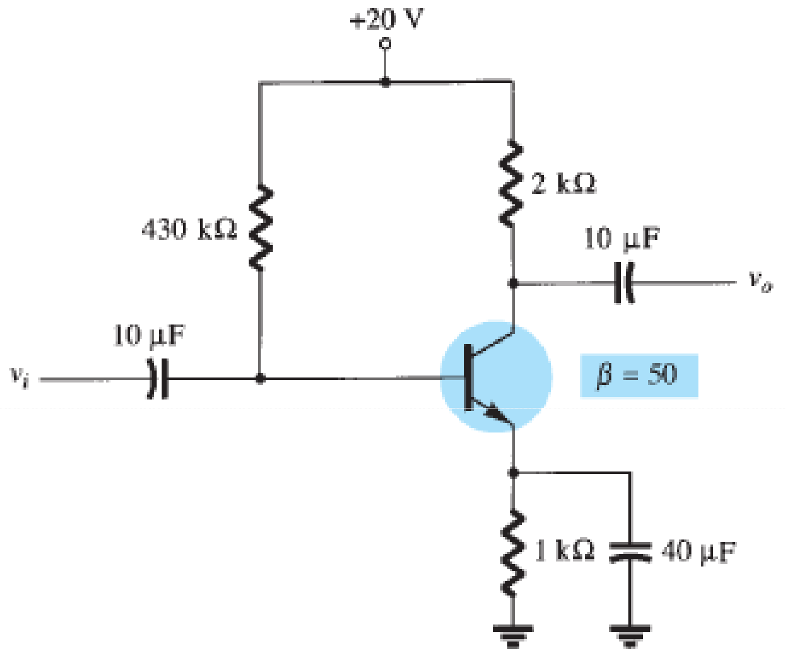
$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{BE} + V_E$$

Example 7

For the following circuit, determine

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.



Solution

Bipolar Junction Transistor

Bipolar Junction Transistor

Example 8

a. Draw the load line for the network of figure (a) on the characteristics for the transistor appearing in figure (b) .
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

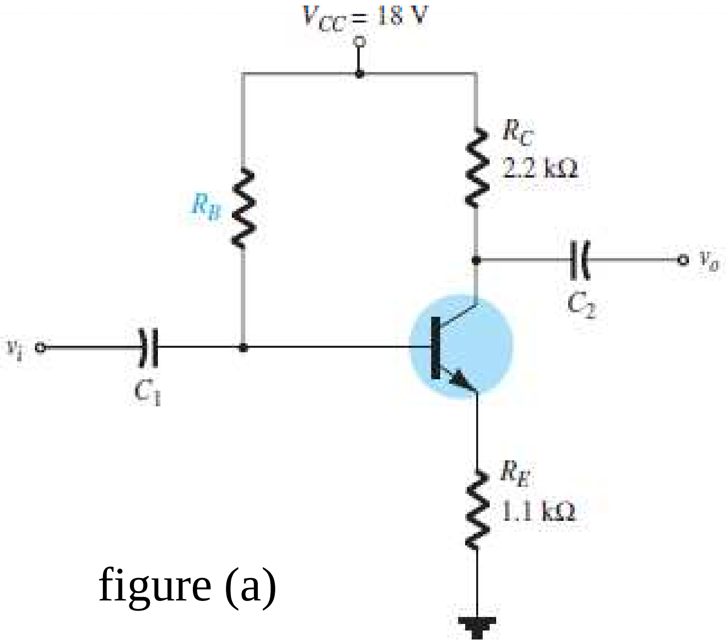


figure (a)

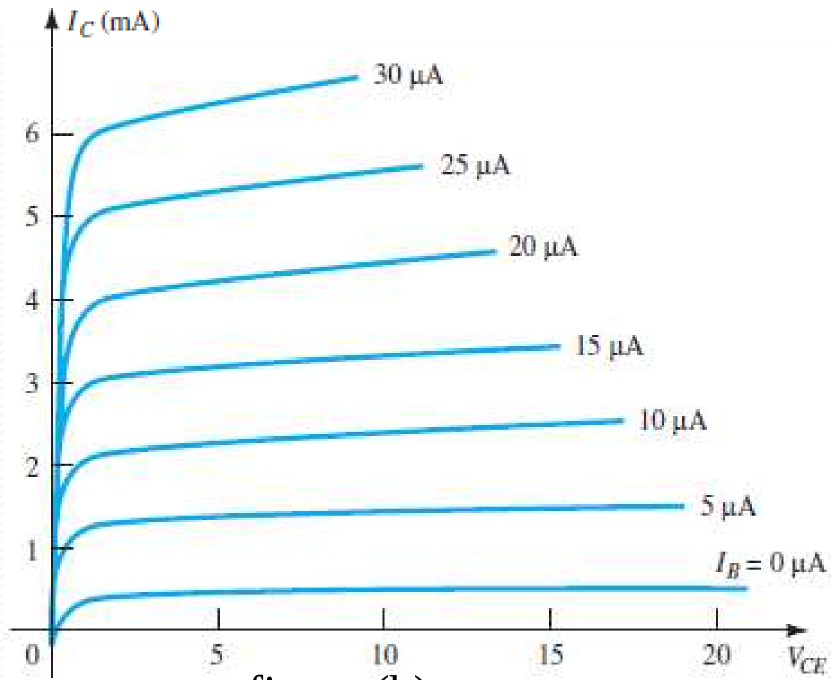


figure (b)

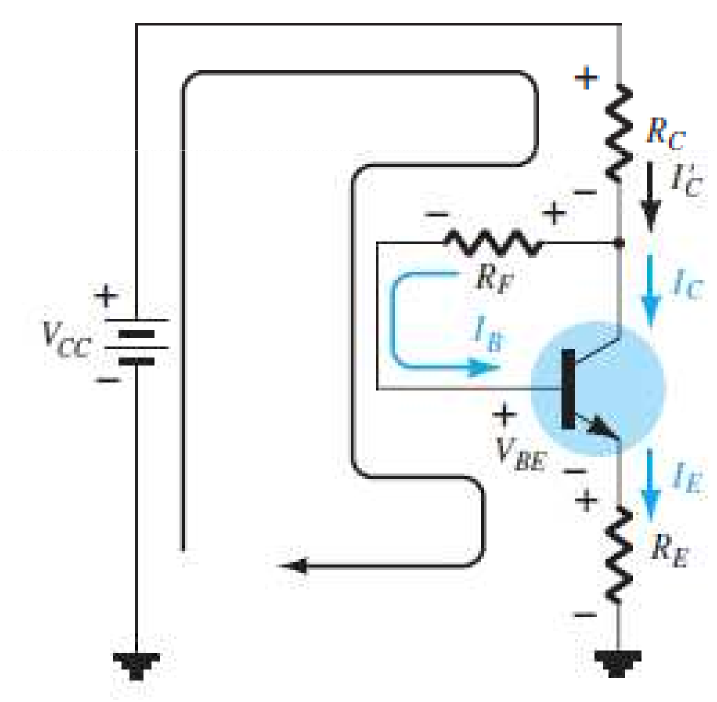
Bipolar Junction Transistor

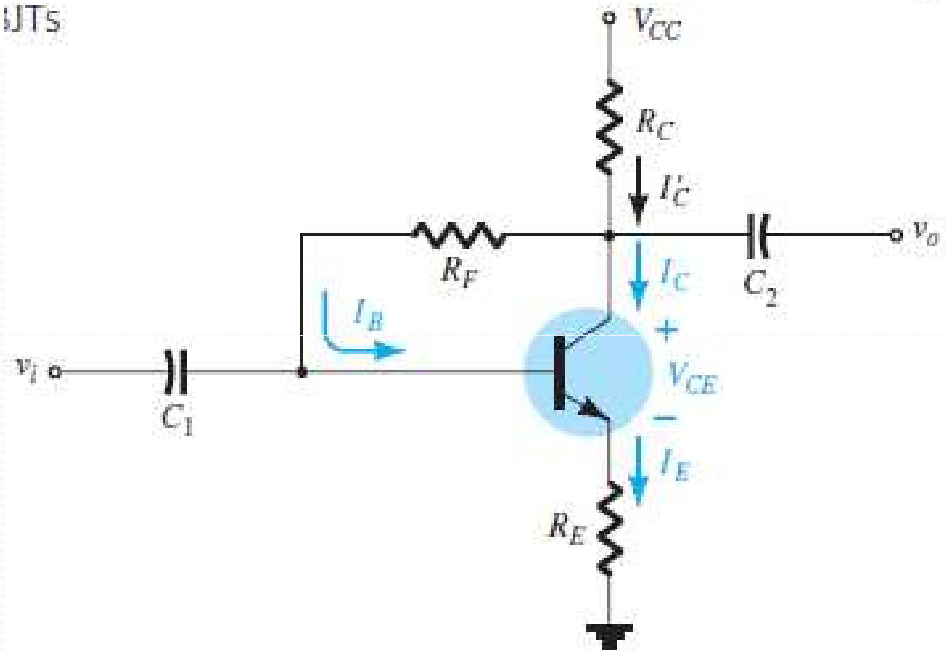
Solution

9.4. Collector Feedback Configuration

An improved level of stability can also be obtained by introducing a feedback path from collector to base

Base–Emitter Loop





$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

(where $I'_C = I_C + I_B$).

Bipolar Junction Transistor

Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

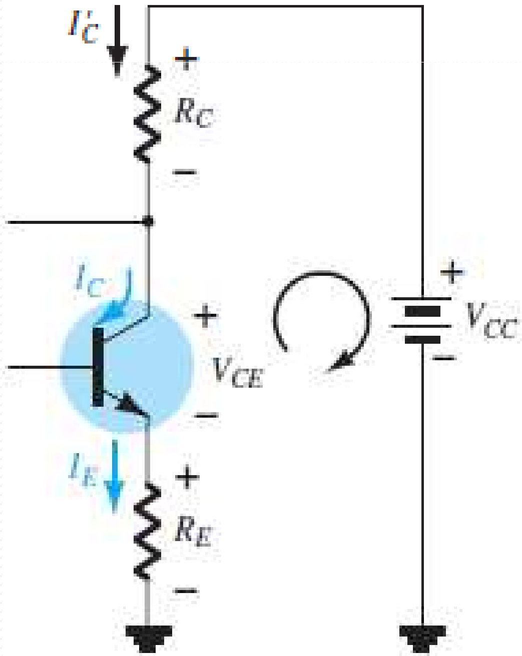
Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

Collector–Emitter Loop



$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Because $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

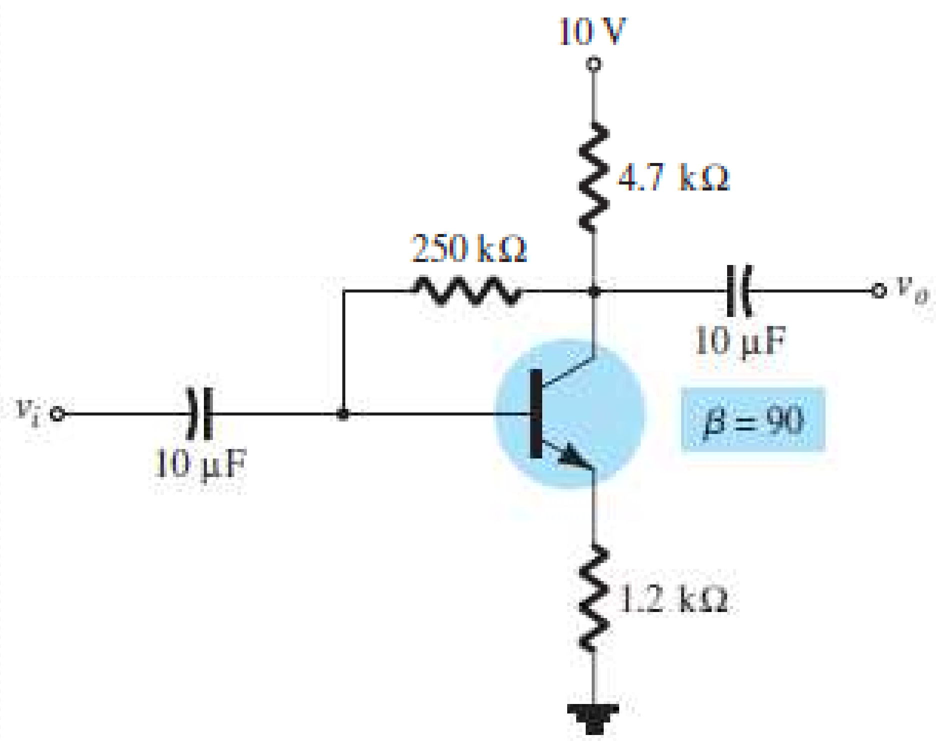
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Bipolar Junction Transistor

Example 9

Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network below

Solution



Example 10

Given the network of Fig. (a) and the BJT characteristics of Fig. (b).

a. Draw the load line for the network on the characteristics.

b. Determine the dc beta in the center region of the characteristics. Define the chosen point as the *Q*-point.

c. Using the dc beta calculated in part b, find the dc value of I_B.

d. Find I_{C_Q} and I_{CE_Q}.

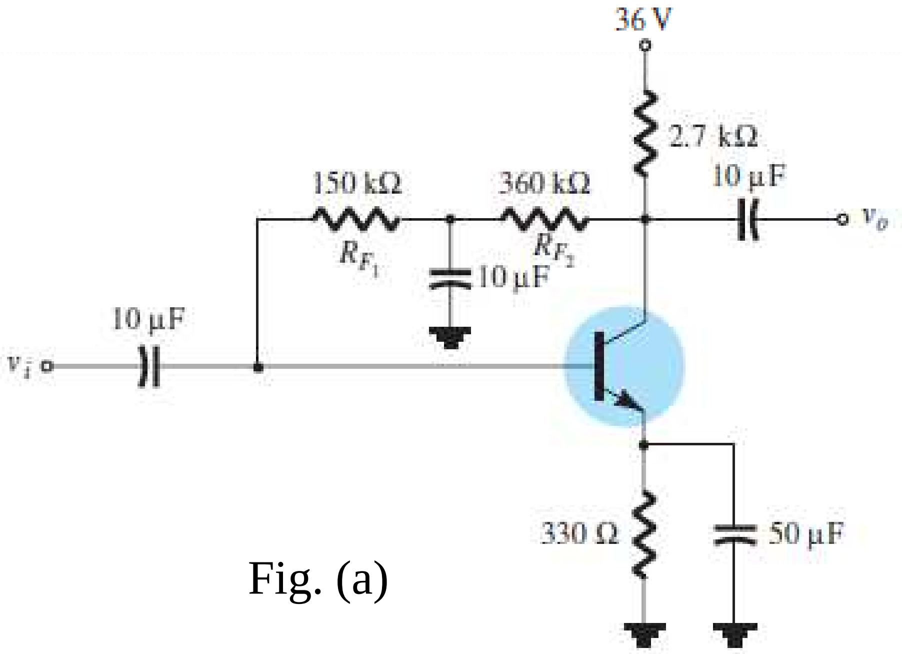


Fig. (a)

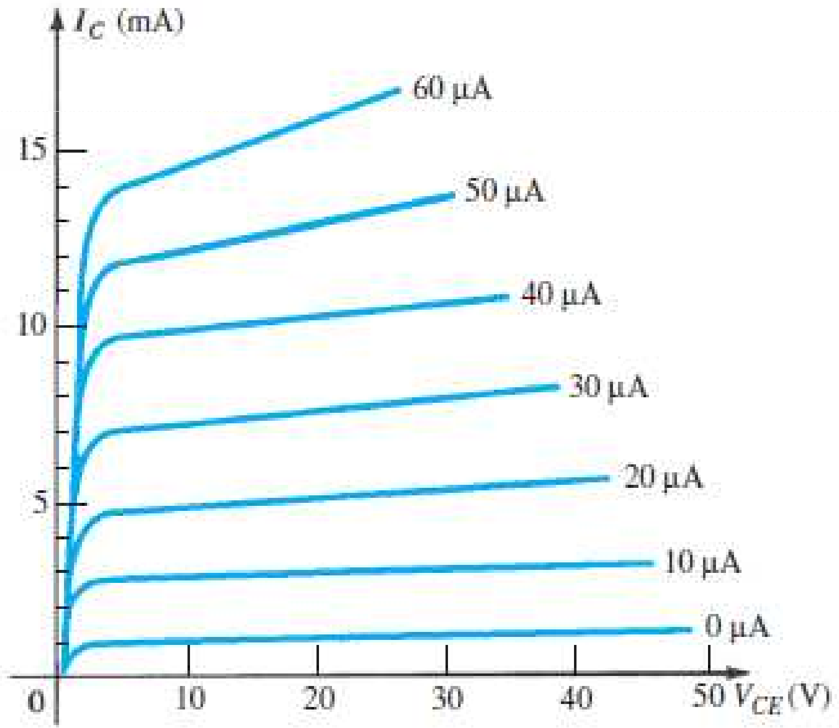


Fig. (b).

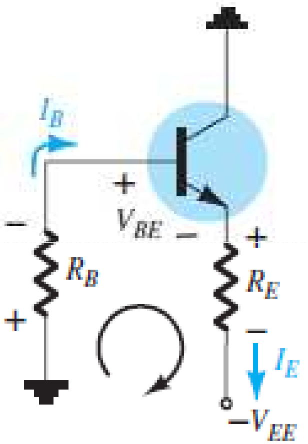
Solution

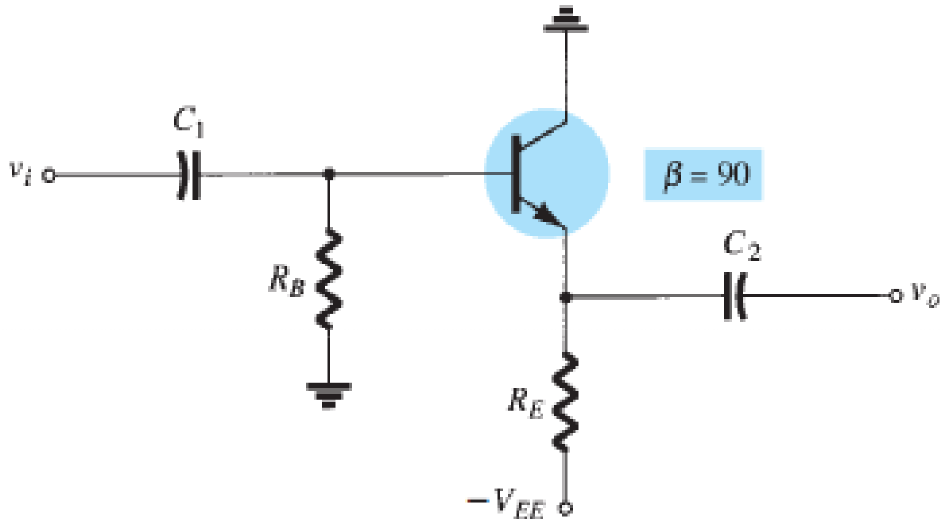
Bipolar Junction Transistor

10. Emitter Follower Configuration

The previous sections introduced configurations in which the output voltage is typically taken off the collector terminal of the BJT.

The dc equivalent of the network





Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

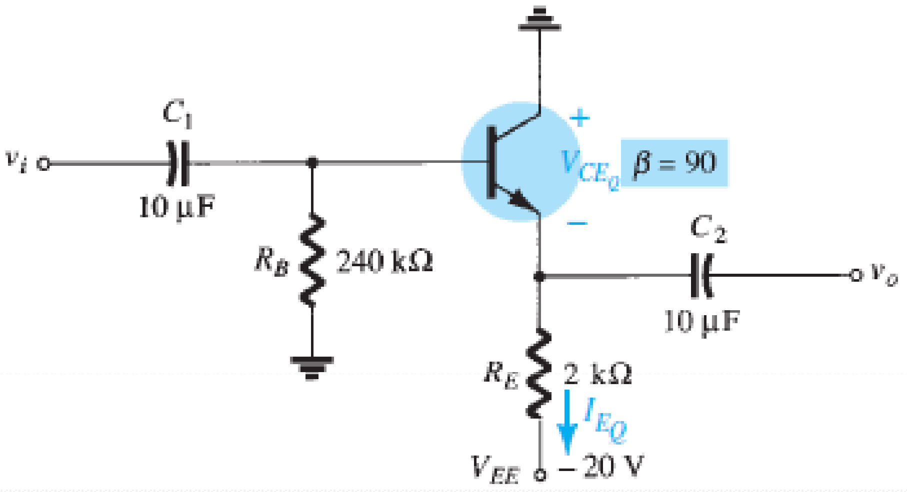
For the output network, an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

Example 11

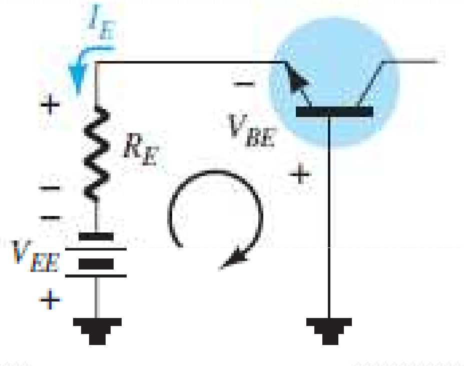
Determine V_{CE_Q} and I_{E_Q} for the network



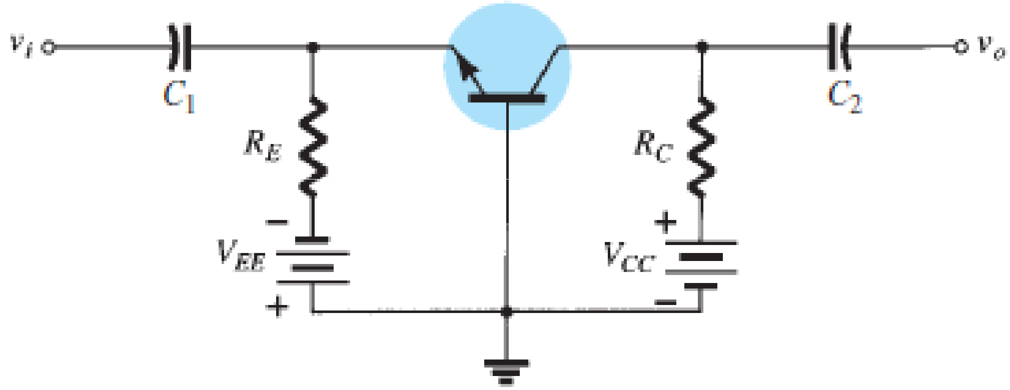
Solution

11. Common-Base Configuration

The common-base configuration is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential.



Input dc equivalent

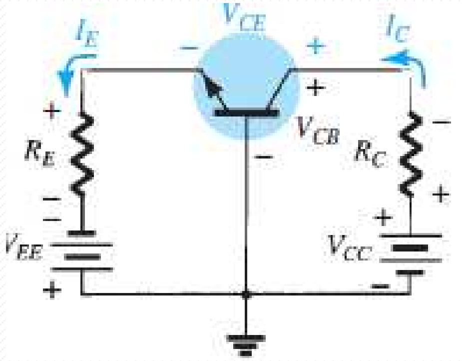


Applying Kirchhoff's voltage law will result in

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Bipolar Junction Transistor



Applying Kirchhoff's voltage law to the entire outside perimeter of the network of Fig. above will result in

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

and solving for V_{CE}: $$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

Because $$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)}$$

The voltage V_{CB} can be found by applying Kirchhoff's voltage law to the output loop

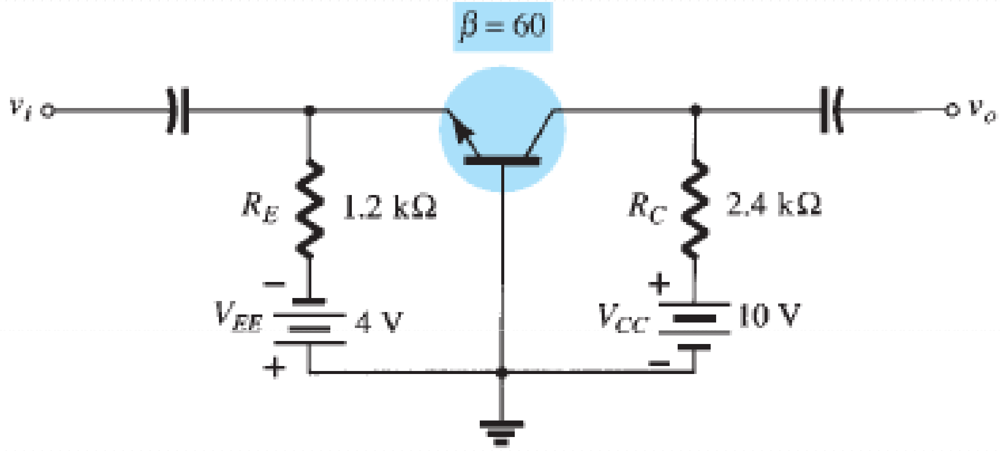
$$V_{CB} + I_C R_C - V_{CC} = 0$$

$$\boxed{V_{CB} = V_{CC} - I_C R_C}$$

Bipolar Junction Transistor

Example 11

Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of the below Fig.



Solution

Bipolar Junction Transistor

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